FOM (Figure of Merit) Analysis for Low Voltage Power MOSFETs in DC-DC Converter

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Abstract - FOM is a generally accepted performance and efficiency indicator for power MOSFETs. However, it is found that the traditional FOM can no longer provide a quick measure of the overall device performance for switched mode power supplies, especially for DC-DC converters using the low voltage (sub-10V) power MOSFETs fabricated in a deep sub-micron CMOS technology. To give a subjective analysis, a new comparison method has been proposed to compare the true overall device performance and power conversion efficiency.

I. INTRODUCTION

In recent years, extensive research activities are being focused in the area of low-voltage (sub-10V) smart power integrated circuits (PICs) for mobile applications. For integrated switch mode power supplies (SMPS), power MOSFETs have become the standard choice for the switching devices. In addition to small chip size, high efficiency and low cost, low output voltage and high current are also important design criteria for the next generation output power stages [1]. However, with a large variety of circuit topologies, switching speeds, load currents, and output voltages, it has become a major challenge to identify the right MOSFET that offers the best performance across a wide range of operating conditions. One of the most popular ways to evaluate the power MOSFETs’ overall performance is to calculate the figure of merit (FOM) which is simply a product of on-resistance (Ron) and total gate charge (Qg).

Since the total power loss is mainly due to both the conduction and gate-drive losses, a small FOM value for power MOSFET generally leads to a high DC-DC converter efficiency. Low voltage power MOSFET fabricated by a deep sub-micron standard CMOS process exhibits a much smaller gate charge and switching delays than those in conventional power MOSFETs [2]. Although this allows the CMOS devices to operate in the MHz range for mobile applications, the traditional FOM becomes less effective in representing the overall device performance due to a relatively small switching loss contribution to the total power loss. The maximum switching frequency of a power MOSFET is mainly limited by its gate charge and switching delays. Therefore, in order to optimize the power MOSFETs for several MHz switching frequency, we need to design for smaller gate charge and input/output capacitances. Fig.1 illustrates the device cross-sectional views of a conventional trench gate power MOSFET and a standard CMOS structure. The parasitic gate source and drain capacitances, Cgs and Cgd are as indicated in both devices. It is evident that the standard CMOS inherently has a much smaller overlap area between its polysilicon gate electrode and n+ source/drain than the conventional trench gate power MOSFET. As a result, CMOS transistor offers a much lower gate capacitance and total gate charge [3].

In this paper, we propose a new FOM that leads to a better indication of the overall performance and power conversion efficiency. For verification purpose, the performance of an output power stage intended for a standard 0.25µm CMOS process technology is studied. Its performance is compared to those designed with a trench gate power MOSFET with similar voltage rating. Although this allows the CMOS devices to operate in the MHz range for mobile applications, the traditional FOM becomes less effective in representing the overall device performance due to a relatively small switching loss contribution to the total power loss. The maximum switching frequency of a power MOSFET is mainly limited by its gate charge and switching delays. Therefore, in order to optimize the power MOSFETs for several MHz switching frequency, we need to design for smaller gate charge and input/output capacitances. Fig.1 illustrates the device cross-sectional views of a conventional trench gate power MOSFET and a standard CMOS structure. The parasitic gate source and drain capacitances, Cgs and Cgd are as indicated in both devices. It is evident that the standard CMOS inherently has a much smaller overlap area between its polysilicon gate electrode and n+ source/drain than the conventional trench gate power MOSFET. As a result, CMOS transistor offers a much lower gate capacitance and total gate charge [3].

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Fig. 1. Cross-sections of conventional trench gate power MOSFET and standard CMOS structures (Both N-Channel).

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II. POWER LOSS ANALYSIS

The power loss analysis of a synchronous buck converter serves as the background for the power loss contributions in DC-DC converters with MOSFET switches. A standard buck (step-down) converter schematic is as shown in Fig. 2. The input supply voltage, $V_{in}$, is stepped down to a regulated output voltage, $V_{out}$. Power MOSFETs are used as both the main switch and the synchronous rectifier, named as high-side switch (HS) and low-side switch (LS), respectively.

![Fig. 2. Synchronous Rectifier Buck Converter](image)

The HS and LS switches are turned on alternatively by the PWM (pulse-width-modulated) signals from a controller with duty ratio, $D$, to achieve the desirable $V_{out}$ at the output of the LC low-pass filter. The power conversion efficiency was calculated using MATLAB Simulink and power loss equations established by Mitter [4]. They are re-stated here with appropriate modifications to describe the buck converter shown in Fig. 2. The overall power loss is the sum of conduction, switching, gate drive, and diode losses. Each contribution is detailed in the following sub-sections.

A. Conduction Loss

Conduction losses due to on-resistance of both the HS and LS switches are functions of the average load current, $I_L$, and the duty ratio, $D$, as shown in equations (1) and (2).

$$P_{cond(HS)} = I_L^2 \cdot R_{ON(HS)} \cdot D$$

$$P_{cond(LS)} = I_L^2 \cdot R_{ON(LS)} \cdot (1 - D)$$

B. Switching Loss

The switching loss due to finite turn-on and turn-off delays ($\tau_{on}$ and $\tau_{off}$) of the power MOSFETs is a function of the drain-source current of the switch, $I_{ds}$, when the device is fully on; the voltage across the switch, $V_{ds}$, when the device is turned off; and the switching frequency, $f_s$, of the PWM control signals:

$$P_{SW} = I_{SW} \cdot V_{SW} \cdot (\tau_{ON} + \tau_{OFF}) \cdot f_s / 2$$

C. Gate Drive Loss

The gate drive loss due to total input gate charge, $Q_g$, of the MOSFET switches is also dependent on $f_s$, of the supply voltage applied to the gate driver, $V_{gg}$.

$$P_{gate} = V_{gg} \cdot (Q_{g(HS)} + Q_{g(LS)}) \cdot f_s$$

D. Diode Loss

To prevent shoot-through, when both the HS and LS switches are on at the same time, deadtime is introduced by the gate control circuitries. During deadtime, both power MOSFETs are off. To maintain a continuous inductor current, the body diode of the LS switch could conduct during this time frame. The total loss due to body diode includes the reverse recovery, $P_{RR}$, and conduction losses, $P_{cond(diode)}$. $P_{RR}$ can be calculated with the reverse recovery charge for a certain technology.

$$P_{diode} = P_{RR} + P_{cond(diode)}$$

Device parameters such as $R_{ON}$ and $Q_g$ are either found from manufacturer’s datasheets or extracted using HSPICE. A converter model along with current program mode control [5] is constructed using MATLAB Simulink to extract the conduction losses and calculate efficiency.

III. SIMULATION RESULTS AND DISCUSSIONS

Low-voltage trench gate power MOSFETs having a similar supply voltage value (sub-10V) as CMOS power output-stage are selected among various conventional MOSFETs. Prior to detailed analysis and discussions on the simulated results, it is important to note that the maximum switching frequencies of conventional power MOSFETs are generally much lower (e.g., < 1MHz) when compared to those for standard CMOS (e.g., from a few MHz to 10MHz). Since the power loss and efficiency are a function of load current, input and output voltages, one should compare the power conversion efficiency at their typical operating conditions in order to analyze their FOM data trends. In Fig. 3, simulated values of the power conversion efficiency are plotted over a range of trench gate power MOSFET with different FOM. As expected, an inversely proportional relationship is observed in all three different operating frequencies: 400, 800, and 1200 kHz. For the conventional trench gate power MOSFETs, the efficiency decreases from 87% to 76% while FOM increases from 156 nC-mΩ to 620 nC-mΩ at $f_s = 800$ kHz.
The power conversion efficiency for a 0.25µm standard CMOS based output-stage is also simulated and plotted with respect to the conventional definition of FOM. As shown in Fig. 4, power conversion efficiency at \( f_S = 10 \) MHz initially increases from 81% to 84% and then slightly decreases back to 81% when FOM increases from 12.4 nC·mΩ to 22.4 nC·mΩ. This clearly indicates that the smaller FOM does not always guarantee a higher efficiency for standard CMOS transistor output stages.

Fig. 4. FOM vs. efficiency for conventional trench gate power MOS.

Since CMOS device structure inherently has smaller total gate charge and capacitances than the trench gate structure, the power conversion efficiency for CMOS output stage is less sensitive to \( Q_g \) or conventional FOMs. This explains why the slope of CMOS data’s trend line is relatively flat when compared to that of trench gate power MOSFETs. A closer look at Fig. 4 shows that the slopes of the curves are dependent on the switching frequency. For example, at \( f_S = 5 \) MHz, the device with FOM = 22.4 nC·mΩ has slightly higher power conversion efficiency than the device with FOM = 12.4 nC·mΩ. Alternatively, at 15MHz, the device with FOM = 12.4 nC·mΩ has a much higher power conversion efficiency. This observation further indicates that for CMOS switches, loss contribution due to \( Q_g \) is small unless we operate the device at a much higher operating frequency. Fig. 5 shows the power loss distribution bar graphs for both trench gate and CMOS devices. Compared to the trench gate power MOSFETs, CMOS output-stages have much smaller total power loss due to a lower output power. In general, contribution of power loss due to total gate charge and switching delay increases as FOM increases.

Fig. 5. Power loss distributions for trench gate power MOSFETs and CMOS.

Fig. 6. Typical Loss Contributions: (a) Trench, (b) CMOS.

Since the traditional FOM is no longer a good indicator of efficiency or power device performance in DC-DC converters, a new FOM is required. This new performance indicator is developed based on two major sources of power loss, namely, \( P_{cond} \) and \( P_{gate} \). The reason for choosing \( P_{cond} \) and \( P_{gate} \) is due to the fact that \( R_{ON} \) and \( Q_g \) are readily available as in conventional power MOSFETs, and the operating conditions required for calculation are also known to the designers. The new FOM has the following form:
From equation (1) and (2), $P_{\text{cond}}$ is proportional to the square of output load current, and by assuming the HS and LS switches have similar $R_{ON}$ as they are usually designed to be, the constant $A$ in equation (7) is the square of the typical output load current. Also, since $f_S$ and $V_{gs}$ are known by the designers prior to choosing power MOSFETs, one can use them along with $Q_g$ to calculate $P_{\text{gate}}$. In order to account for both the $Q_g$ of HS and LS switches, it is necessary to note that $Q_g$ of a PMOS switch is about 3 times larger than that of an NMOS. Due to hole-electron mobility ratio, and in order to have similar $R_{ON}$ for both the HS and LS switches, it is necessary to note that $Q_g$ of a PMOS switch is about 3 times larger than that of an NMOS. Therefore, the total $Q_g$ is about 4 times $Q_{g\text{LS}}$. This is reflected in the definition for the constant $B$ in equation (8). The new FOM is plotted in Fig. 7 along with the traditional FOM, and converter efficiency.

IV. CONCLUSION

Various power loss mechanisms and overall efficiency of a synchronous DC-DC buck converter with power MOSFETs based on 0.25µm standard CMOS process technology have been analyzed. In contrast to the conventional trench gate power devices, the low voltage CMOS-based output-stage has different efficiency trend with respect to the conventional FOM. Therefore, a new FOM has been proposed to model specifically the switching mechanism of DC-DC converters and the power loss distribution for CMOS output-stages. This new FOM can serve as a useful tool for CMOS power-stage designers.

Table 1. Data comparison for current and future power MOSFETs used in low voltage dc-dc converter

<table>
<thead>
<tr>
<th>Technology</th>
<th>Efficiency (%)</th>
<th>$P_{\text{cond}}$ (W)</th>
<th>$P_{\text{gate}}$ (W)</th>
<th>$Q_g$ (nC)</th>
<th>$f_S$ (MHz)</th>
<th>$W_{\text{total}}$ (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trench MOSFET from VISHAY</td>
<td>86.6</td>
<td>199</td>
<td>6.0</td>
<td>10</td>
<td>50</td>
<td>10</td>
</tr>
<tr>
<td>Trench MOSFET from VISHAY</td>
<td>82.1</td>
<td>123</td>
<td>6.0</td>
<td>10</td>
<td>50</td>
<td>10</td>
</tr>
<tr>
<td>TSMC 20um Standard CMOS</td>
<td>85.7</td>
<td>100</td>
<td>6.0</td>
<td>10</td>
<td>50</td>
<td>10</td>
</tr>
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REFERENCES