Abstract - A trenched LOCOS process has been applied to a UMOS structure to reduce the gate-to-source overlap capacitance ($C_{gs}$). A 40% reduction in $C_{gs}$ is achieved comparing to conventional UMOS, and the device's specific on-resistance $R_{on,sp} = 60 \text{m} \Omega \cdot \text{mm}^2$ is observed. The improvement in device figure-of-merit (FOM = $R_{on} \times Q_g$) is about 58%.

I. Introduction

The power semiconductor industry has achieved rapid progress in the reduction of on state resistance and switching losses in power MOSFETs, especially in the low voltage range such as 60-70V rating for automotive applications [1]. Trench MOSFET (UMOS) is particularly attractive in these applications. In order to further reduce $R_{on,sp}$ and switching loss, in this paper, we propose a new technology, trenched LOCOS process for the gate oxidation.

II. Device Structure

A typical UMOS structure is as shown in Fig.1. The device trench depth is 2μm, and the width is 1μm. The rightmost part of the device is the device termination. The dark region in the p-body represents heavy boron concentration. We used the hexagonal shape in the layout in order to maximize the area utilization efficiency, as shown in Fig. 2.

A comparison of the device structures between the proposed trenched LOCOS UMOS and the conventional UMOS is as shown in Fig. 3. Using the trenched LOCOS technique, the oxide at the shoulder of the UMOS is much thicker than that in the conventional UMOS. The circle indicates the difference between conventional UMOS and trenched LOCOS UMOS. The trenched LOCOS UMOS exhibits vertical bird’s beaks at the trench shoulders.

In this paper, the fabrication process and device structure have been developed by using the TCAD tools (Tsuprem4 and Medici). The devices were fabricated by Asahi Kasei Microsystems Co. Ltd. (AKM) using a 0.35μm process. The proposed device exhibits a better tradeoff between specific on-resistance and gate input capacitance. The device ruggedness is also found to be comparable to conventional devices.

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Fig. 1. UMOS full structure with termination.

Fig. 2. Micrograph of the die (hexagonal cell).

Fig. 3. (a) Conventional UMOS, (b) Trenched LOCOS UMOS.
III. Fabrication Process and Results

The device fabrication is based on a 7 µm n-type epitaxial layer with phosphorus doping of $5 \times 10^{15}$ cm$^{-3}$ on top of a heavily As-doped n$^+$ <110> substrate [2]. Boron and arsenic implantation of $3 \times 10^{15}$ cm$^{-2}$ at 120keV and $3 \times 10^{15}$ cm$^{-2}$ at 100keV were used to produce the p-well and n$^+$ source, respectively.

Thereafter, a 2µm deep and 1µm wide U-shaped trench was dry etched and the trenched LOCOS process was carried out to form a thick oxide layer at the trench sidewall. The Si$_3$N$_4$ deposition and etch back leaves open area to form LOCOS at trench bottom, and at trench shoulders (see Fig. 4). This process is simpler and easier to control when compared to the approach of oxide deposition and etch back introduced by Takaya et al. [3].

After nitride removal and a brief sidewall oxide cleaning, gate oxidation at 950°C was performed to form a 600 Å gate oxide on the trench wall. As visualized in simulation, this relatively high temperature oxidation causes some segregation of boron and phosphorus at the oxide and epitaxial layer interface, which reduces the effective channel length, this also helps to reduce the device $R_{on}$. On the other hand, the sidewall gate oxide thickness is increased at the top part of the UMOS due to the trenched LOCOS process. This thick oxide at the n$^+$ source decreases $C_{gs}$ significantly.

In order to pinpoint the breakdown location to be at the center of the p-body/n-epi junction, a second high energy boron ion implantation through the body contact hole is carried out.

Finally, a deep body source contact [4] was formed by shallow trenched Si etch and p$^+$ boron implantation, because deep body source contact can greatly reduce the contact resistance, as indicated in Fig. 5.

![Si$_3$N$_4$ deposition, Dry etch, LOCOS](image1)

![Conventional LOCOS process vs. trench LOCOS process](image2)

**Fig. 4.** (a) Schematic of the trenched LOCOS process to form thick oxide layers at trench bottom and shoulders. (b) A SEM cross sectional view of the UMOS structures fabricated by conventional and trenched LOCOS process. Segregation reduces the effective channel length.

![Measured breakdown I-V curve of trenched LOCOS UMOS with and without p$^+$ (2) boron implantation](image3)

**Fig. 5.** Schematic of p$^+$ (2) boron implantation and deep body source contact formation.

![Measured breakdown I-V curve of trenched LOCOS UMOS with and without p$^+$ (2) boron implantation](image4)

**Fig. 6.** Measured breakdown I-V curve of trenched LOCOS UMOS with and without p$^+$ (2) boron implantation.
IV. Experimental Results and Discussions

A plot of the breakdown characteristics of the LOCOS UMOS is presented in Fig. 6. The solid line is the breakdown curve without the additional p⁺ boron implantation. In this case, the breakdown will occur near the gate oxide, which is undesirable for power devices. With the second p⁺ boron implantation, the electric field will be localized near the p-body and n-epi junction, and breakdown will occur at the bottom of p-body, which is more desirable for the power UMOS.

### Table I

<table>
<thead>
<tr>
<th>Device characteristics of conventional UMOS and trenched LOCOS UMOS</th>
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<tbody>
<tr>
<td>Device (Area: 1 mm²)</td>
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<tr>
<td>----------------------</td>
</tr>
<tr>
<td>BV_{th} at I_{th}=1uA, V</td>
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<tr>
<td>BV_{th} at I_{th}=250uA, V</td>
</tr>
<tr>
<td>R_{on,sp} at V_{gs}=10V, I_{ds}=100mA, mΩ mm²</td>
</tr>
<tr>
<td>C_{gs} at V_{ds}=0V, pF</td>
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<tr>
<td>C_{gd} at V_{ds}=0V, pF</td>
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<tr>
<td>C_{di} at V_{ds}=0V, pF</td>
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<tr>
<td>Q_{g} at V_{gs}=10V, nC</td>
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<tr>
<td>FOM (R_{on} \times Q_{g}), nC·mΩ</td>
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</tbody>
</table>

The most prominent improvement is the reduction in C_{gs}, 432pF comparing to 722pF for the conventional UMOS. This is primarily due to the increase in the oxide thickness at the n⁺ source. Another important improvement is the specific on-resistance, which is almost half of the conventional UMOS. This phenomenon can be due to the high temperature trenched LOCOS process that causes boron and phosphorus segregation at the oxide and epitaxial layer interface. This results in a shorter effective channel length.

Gate charge test has also been carried out to quantitatively determine the charge reduction in new structure UMOS. The circuit used for gate charge test is as shown in Fig. 9.

![Gate charge test circuit](image)

### Fig. 8. Measured gate charge characteristics of trenched LOCOS UMOS and conventional UMOS.

- **Phase 1**
  - Q_{gs}
  - Q_{gd}
  - Q_{g}

- **Phase 2**
  - Q_{gs}
  - Q_{gd}
  - Q_{g}

- **Phase 3**
  - Q_{gs}
  - Q_{gd}
  - Q_{g}

**Fig. 7. Measured characteristics of trenched LOCOS UMOS**

The measured I-V characteristics are as shown in Fig. 7. The LOCOS UMOS achieved a breakdown voltage of 60V and R_{on,sp} = 85mΩ mm² at V_{gs} = 3.5V. At V_{gs} = 10V, R_{on,sp} = 60mΩ mm².

A comparison of measured electrical characteristics between conventional UMOS and trenched LOCOS UMOS are presented in Table 1.
The upper power MOSFET is used as a current regulator to set the drain current. The gate source \( V_{gs} \) is 10V, and the \( V_{dd} \) is set to be 40V. Phase 1 in Fig. 8 represents a linear increase in \( V_{gs} \) with gate charge. \( Q_{gs} \) defines the charge needed during turn on. In phase 2, \( V_{gs} \) remains relatively constant, and the drive current starts to charge the Miller capacitance, \( C_{pd} \). During phase 3, the gate capacitance is the summation of \( C_{gs} \) and \( C_{gb} \) and the total charge is \( Q_g = Q_{gs} + Q_{gb} \), which is required to charge gate to \( V_{gs} = 10V \).

Under this condition, the \( Q_{gs} \) is 23% less for trenched LOCOS UMOS. Overall, the FOM \( (R_{on} \times Q_g) \) has been improved by 58% without compromising the breakdown voltage.

\[
\frac{FOM_{Conventional} - FOM_{LOCOS}}{FOM_{Conventional}} = \frac{1639 - 684}{1639} = 58\%
\]

High speed switching, would induce a lot of stress on the device, which might lead to device damage. This occurs especially when switching with an inductive load. The rapid turn off of an inductive load can cause avalanche breakdown of the drain to source diode, resulting from \( V_{ds} \) transients. [5]

In order to determine the ruggedness of the new device, the Unclamped Inductive Switch (UIS) test was carried out for the trenched LOCOS UMOS.

\[ \text{Fig. 10. The circuit used for UIS test.} \]

When the gate voltage is switched off, there is still an inductor current flowing through the circuit as maintained by the collapsing inductive field. This current forces the internal diode of the MOSFET into avalanche breakdown. If the current is too large for the device to handle, the device will be permanently destroyed. The inductor used for UIS test in Fig. 10 is 1.09mH. From the UIS test results (Fig. 11), the trenched LOCOS UMOS process demonstrates comparable ruggedness as conventional UMOS. This is because the overall process does not involve any doping change within the p-body or n-epi junction. The parasitic BJT inherent in the UMOS remains same.

\[ \text{Fig. 11. UIS test results of UMOS devices fabricated by conventional and trenched LOCOS process.} \]

V. Conclusions

A novel trenched LOCOS UMOS technique has been proposed and experimentally verified. This technique is easy to carry out and the new device exhibits 40% reduction in \( C_{gs} \), 58% improvement in FOM when compared to conventional device. The new device illustrates comparable ruggedness as the conventional devices without compromising the breakdown voltage.

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