High Performance Low-Voltage Power MOSFETs with Hybrid Waffle Layout Structure in a 0.25µm Standard CMOS Process

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Summary
This paper reports on a low-voltage CMOS power MOSFET layout technique, implemented in a 0.25µm, 5-metal-layer standard CMOS process that is suitable for multi-MHz integrated switched mode power supplies. The proposed hybrid waffle (HW) layout technique organizes MOSFET fingers in a square grid (or waffle) arrangement. It is designed to provide a trade-off between the width of diagonal source/drain metal and the active device area, allowing more effective optimization between switching and conduction losses. In comparison with conventional multi-finger (MF) layouts, the HW layout is found to exhibit a 30% drop in overall on-resistance with 3.6 times smaller total gate charge for CMOS devices with a current rating of 1A. Integrated DC-DC converters using HW push-pull output stages are found to have higher simulated power conversion efficiencies at switching frequencies beyond multi-MHz.

Motivation
Today’s integrated DC-DC converters require low-voltage power devices with low on-resistance ($R_{ON}$) and low gate charge ($Q_G$) to provide good power conversion efficiency in the multi-MHz (>5MHz) range. Since the conduction and switching losses are dependent on the on-resistance ($R_{ON}$) and total gate charge ($Q_G$), it is necessary to minimize both parasitic resistance and capacitance as illustrated in Fig. 1. Traditionally, large CMOS transistors are designed with MF layout structure (see Fig. 2) to maximize the channel width (W) per unit area (A). Waffle layout design was introduced to further improve the W/A ratio by sharing each source/drain contact with four neighboring transistors. This layout structure was able to offer a lower $R_{ON}$ with a higher W/A ratio. However, the MF and waffle layout approaches cannot satisfy high switching frequency, output current and power conversion efficiency, simultaneously. Large parasitic interconnect resistances and capacitances arising from the narrow metal and polysilicon line width and spacing are the limiting factors.

Results
At first inspection, the HW layout, as show in Fig. 3(a), appears to have sub-optimal use of silicon area. Much of the layout is occupied by metal interconnection rather than active area. However, the wider metal interconnection can actually lower the overall on-resistance of the power transistor. This is especially critical for large devices where the metal resistance is comparable to the channel resistance. The reduced overall W also results in lower gate and parasitic junction capacitances. The width of each transistor segment will determine the size of the waffle and consequently the trade-off between $R_{ON}$ and $Q_G$. Fig. 2 and 3 illustrate the layouts and extracted circuit models for the MF and HW structures, respectively. Parasitic resistances from each physical design layer were considered in these circuit models. The gate charge waveforms for both MF and HW structures are as shown in Fig. 4. The change in $I_{DS}$ only affects $Q_{GS}$ rather than $Q_{GD}$. The total $Q_G$ for the HW structure is 3.6 times smaller than that for the MF structure at $V_G = 3.3V$. This is due to the fact that the total W for the MF structure is more than 3 times wider when compared to a HW structure with the same active area. Fig. 5 illustrates $R_{ON}$ and $Q_G$ trends for the MF and HW structures as a function of area. The $R_{ON}$ trends for MF and HW structures cross over at $Area = 0.066 \text{ mm}^2$. This indicates that the HW structure can achieve smaller overall $R_{ON}$ even though its overall W is 3 times narrower than the MF layout. Finally, the power conversion efficiencies as a function of switching frequency, $f_{sw}$ for different load currents are compared in Fig. 6. The HW structure can offer higher power conversion efficiencies at both light loads and high switching frequencies. This performance gain can be achieved based on layout techniques with no process change, and will be very attractive for future low voltage integrated DC-DC converter designs.

Fig. 1: Parasitic effects: (a) On-resistance and (b) Gate charge reduction trends

Fig. 2: Multi-fingers structure: (a) Layout and (b) extracted circuit model

Fig. 3: Hybrid waffle structure: (a) Layout and (b) extracted circuit model
Fig. 4: Gate charge characteristics of (a) Multi-fingers and (b) Hybrid waffle structures.

Fig. 5: R\textsubscript{ON} and Q\textsubscript{G} plots as a function of MF and HW power MOSFET active areas.

Fig. 6: Comparison of power conversion efficiencies for both MF and HW structures as a function of switching frequency and for different load currents.