A 0.02 nJ Self-calibrated 65nm CMOS Delay Line Temperature Sensor

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***Abstract*—This paper presents an area and power efficient delay line based temperature sensor for on-chip monitoring. This sensor can be deployed in large numbers on a microprocessor chip to facilitate advanced thermal and power management techniques. The proposed self-calibration design eliminates the effort associated with two-point calibration commonly found in conventional temperature sensors. In addition, it saves digital decoding power by the use of both tab and counter decoding. Measurement results for a 65nm CMOS design show that the proposed temperature sensor consumes 0.02 nJ energy per conversion. It occupies an active area of 0.002 mm^2 and has a resolution of 0.5 °C with errors within ±2.0 °C over a temperature range from 20 to 80 °C.**

I. INTRODUCTION

Modern nano-meter scale VLSI technology has advanced to a point where the amount of power consumed in a typical microprocessor chip under maximum performance situation could cause overheat and even become destructive. The elevated chip temperature can cause problems ranging from increased leakage power, malfunctioning to physical damage of the silicon die and the package. As a result, both dynamic power and dynamic thermal management, which rely on accurate thermal information obtained from integrated sensors, are necessary. For example, AMD's Opteron microprocessor utilizes 38 temperature sensors as part of its thermal management system [1].

As process variation increases with technology scaling, more hotspots need to be monitored on a chip. Therefore, the integrated temperature sensor arrays should introduce minimum area and power overhead. Delay line based temperature sensors [2]-[8] consume less power and area when compared to the traditional bandgap voltage based counterparts [9]. The delay line temperature sensor reported by Chen *et al.* relies on two delay lines, one for temperature-to-time sensing conversion and another for time-to-digital conversion (TDC) [2]. However, the TDC relies on carefully sized circuitry to ensure a small temperature coefficient. Another previously published delay line temperature sensor [3] consists of a MOSFET PTAT (Proportional to Absolute Temperature) voltage source followed by a chain of current controlled delay cells. This design requires a resistor, and the MOSFET PTAT is subject to mismatches that deteriorate with technology scaling. A ring oscillator is employed to realize direct temperature to digital conversion in [4] and [5], thus avoiding the intermediate conversion of the signals in time or voltage domain. However, in [4] a much higher frequency is required to calibrate the oscillation frequency. In [5], the output frequency versus temperature characteristic exhibits a large nonlinearity. The counter employed to digitalize the temperature dependent frequency consumes continuous dynamic power. To accommodate for mass production, one-point calibration [2], [6] and auto-calibration [8] are proposed to replace the traditional two-point calibration [7]. The auto-calibration is performed by correlating measurement results with simulation results in [8]. Its accuracy is dependent on the validity of the spice model. In addition, process variations are subject to doping fluctuations, gate-oxide thickness and line edge roughness variations. All the above factors are difficult to predict, especially as technology scales. This paper proposes a ring oscillator (RO) based temperature sensor with self calibration and low power consumption. It can also be easily ported to future generations of technology. Section II introduces the sensor architecture, operating principle, power saving method and self-calibration methodology. Measurement results are discussed in section III, followed by a brief conclusion in section IV.

II. OPERATING PRINCIPLE

A. Temperature dependent frequency

The proposed temperature sensor as shown in Fig.1 (a) can be divided into three parts: the main ring oscillator and its decoding circuitry; the auxiliary ring oscillator and its decoding circuitry; and the self-calibration algorithm block. The main and the auxiliary ring oscillators generate CTAT (Complementary to Absolute Temperature) and PTAT frequencies, respectively. Both proportional to temperature frequencies are quantized into 12 bits digital outputs and are compared in the self-calibration block, which generates an 8 bit calibrated digital output as a representation of the temperature. The gate-control voltage level for the auxiliary

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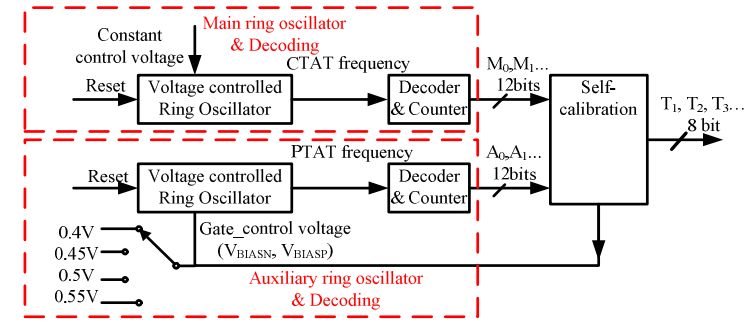
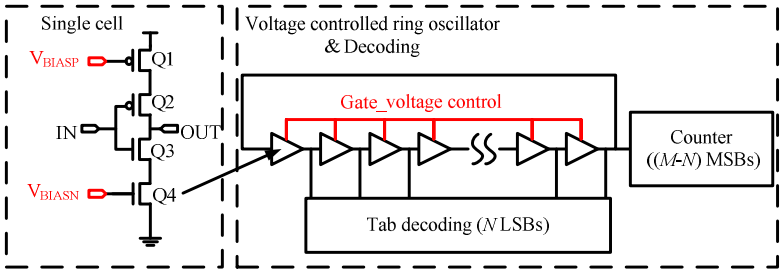


(a)Overall design architecture



(b) Single cell and decoding

Figure 1. Proposed overall and single cell design architecture.

ring oscillator is also adjusted by the self calibration block. The individual delay cell in both voltage controlled ring oscillators is as shown in Fig. 1 (b): in the main ring oscillator, $V_{BIASN} = V_{DD}$, $V_{BIASP} = GND$, and transistor Q2 and Q3 function as a pair of logic inverter. It has been demonstrated that the propagation delay of a logic gate has a positive temperature coefficient [2], [7], where the transistors operate in both linear and saturation regions. Therefore, the ring oscillator frequency, which is inversely proportional to the propagation delay, is a CTAT frequency. In the auxiliary ring oscillator, Q4's gate-control voltage V_{BIASN} is set to be just above the threshold voltage and its drain current can approximated as [3]:

$$I_{ds} = \mu \cdot C_{OX} \cdot \frac{W}{L}\left(\frac{kT}{q}\right)^2 \exp\left[\left(V_{BIASN} - V_{TH}\right)/(nkT/q)\right]$$
$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{-\alpha_u}, \alpha_u = 1 \sim 3 \qquad (1)$$
$$V_{TH}(T) = V_{TH}(T_o) - \alpha_v (T - T_0)$$

where α_μ and α_v are the temperature coefficient of mobility and threshold voltage, respectively. They are treated as constants in this analysis. Taking the derivative of (I_{ds}/T):

$$\frac{\partial\left(\frac{I_{ds}}{T}\right)}{\partial T} = m\left[a\left(V_{BIASN} - V_{TH}\right)^2 + b\left(V_{BIASN} - V_{TH}\right) + c\right]$$
$$m = -T^{-\alpha_\mu} \exp\left(\frac{V_{TH} - V_{BIASN}}{nV_T}\right) \qquad (2)$$
$$a = \frac{k}{q}; b = -\alpha_v V_T; c = \left(\alpha_\mu - 1\right) e n^2 V_T^3$$

where (I_{ds}/T) is constant when its derivative (2) is equal to zero:

$$a\left(V_{BIASN} - V_{TH}\right)^2 + b\left(V_{BIASN} - V_{TH}\right) + c = 0 \qquad (3)$$

$(V_{BIASN} - V_{TH})$ is solvable as $b^2 >> 4ac$ in (3) and V_{BIASN} depends on the threshold voltage V_{TH} which decreases with temperature. Therefore, a certain V_{BIASN} value results in a (I_{ds}/T) ratio with small variation over a certain temperature range. The same analysis also holds for V_{BIASP}. This is verified using Spectre model for TSMC's 65nm technology as shown in Fig. 2. As Q4's current controls the auxiliary ring oscillator's frequency, its output codes are directly proportional to temperature when its gate-control voltage V_{BIASN} satisfies equation (3). From Fig. 2, when the value of V_{BIASN} is smaller than that specified by (3), (I_{ds}/T) increases with temperature; when V_{BIASN} is larger than that specified by (3), (I_{ds}/T) decreases with temperature as the transistor's operating region moves from sub-threshold to linear. This is the basis for self-calibration in Part *C*.

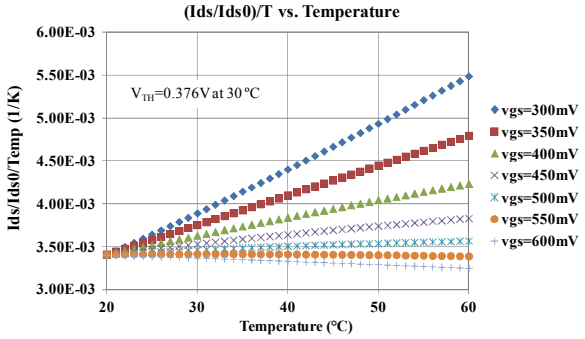


Figure 2. Drain current Ids over temperature ratio using Spectre model for TSMC's 65nm technology.

B. *Power saving decoding*

The temperature dependent frequency from the ring oscillator is quantized by a traditional counter as in [5]. The

total dynamic power and energy per conversion consumed by the ring oscillator and the counter can be expressed as:

$$P_{dyn} = P_{dyn\_ringoscillator} + P_{dyn\_counter} = V_{DD} \cdot i_{ave} + V_{DD} \cdot i_{ave} \cdot \frac{C_{counter}}{C_{inverter} \cdot N_{stage}} \quad (4)$$

$$E = P_{dyn} \cdot \frac{1}{f_s} = V_{DD}^2 \cdot \left(C_{inverter} + \frac{C_{counter}}{N_{stage}} \right)$$

where V_{DD} is the supply voltage; i_{ave} and $C_{inverter}$ are the average charging or discharging current and the gate node capacitance in a single inverter cell; N_{stage} is the number of inverter cells in the ring oscillator; $C_{counter}$ is the capacitance at register's inputs of the counter . Equation (4) indicates that larger gate node capacitance and smaller average current in the inverter will result in lower power consumption [5]. On the other hand, larger node capacitance actually increases energy per conversion while smaller controlling current doesn't affect energy per conversion. If N_{stage} (the number of delay cells in ring oscillator) increases, both dynamic power and energy consumed by the counter decrease as it is counting at a slower frequency. To maintain the same resolution, tab decoding in ring oscillator is employed: as shown in Fig.1 (b). The decoder detects the position where the reset pulse stops within the delay line and converts the thermal code to binary code. The counter calculates the number of pulses at the end of the ring oscillator. The counter produces the (*M*-*N*) MSBs and the decoder decodes the *N* LSBs. Therefore, the dynamic power and energy consumption are reduced by a factor of 2^N.

C. *Self-calibration*

The value for V_{BIASN} in (3) is deduced by comparing the auxiliary ring oscillators' frequencies at three different temperatures (one at room temperature, and two other unknown temperatures that are initially measured and then verified). As shown in Fig. 3, initially at an equilibrium temperature T_0 (e.g. room temperature), the digital outputs M_0 from the main ring oscillator and A_0 from the auxiliary ring oscillator are stored. When temperatures are changed to T_1 and T_2 due to normal operation of the VLSI chip that is being monitored, the digital outputs M_1, M_2 from main ring oscillator and A_1, A_2 from auxiliary ring oscillator are captured. Assuming that equation (3) is satisfied:

$$\frac{A_1}{T_{A1}} = \frac{A_0}{T_0} \quad (5)$$

The main ring oscillator outputs are assumed to be linear, with slope equal to:

$$\frac{M_2 - M_0}{M_1 - M_0} = \frac{T_{M2} - T_0}{T_{A1} - T_0} \quad (6)$$

The only two unknowns in (5) and (6) are temperatures T_1 and T_2. If the auxiliary ring oscillator gate-control voltage is as specified in (3), then the A_2/T_{M2} ratio equals to that in (5). Otherwise, if $A_2/T_{M2} > A_0/T_0 = A_1/T_{A1}$, it means that ($I_{ds}$/*T*) in the auxiliary ring oscillator increases with temperature. This indicates a smaller V_{BIASN} than expected (as shown in Fig.2). In this case V_{BIASN} should be increased. As V_{BIASP} controls the charging current for Q2 as shown in Fig 1.(b), it should be decreased accordingly. After the auxiliary ring oscillator gate-control voltage level is selected, the gain and offset of the main ring oscillator are calibrated as $(T_{A1}-T_0)/(M_1-M_0)$ and $(T_{A1}\times M_0-M_1\times T_0)/(M_0-M_1)$, respectively, and the auxiliary ring oscillator can be turned off. In normal operation, the temperature *T* is calculated from the output *M* of the main ring oscillator as:

$$T = \frac{T_{A1} - T_0}{M_1 - M_0} \times M + \frac{T_{A1} \times M_0 - M_1 \times T_0}{M_0 - M_1} \quad (7)$$

The self-calibration algorithm block is synthesized from Verilog code using Encounter tool and can be shared among all sensors on the same chip.

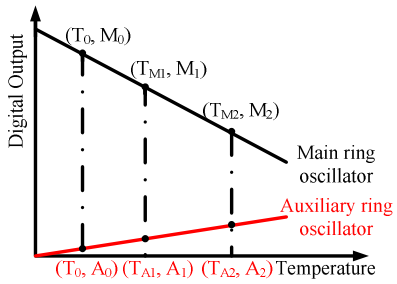


Figure 3. The characteristics of the main and auxiliary oscillators for the self-calibration methodology.

III. Measurement Results and Discussion

An experimental design as shown in Fig. 1 is implemented using TSMC's 65nm CMOS technology. Measured digital codes from the main and auxiliary ring oscillators for three test chips are as shown in Fig. 4. The temperature is measured between 20 °C to 80 °C, which is the range of interest for the on-chip thermal sensing. Measured calibrated digital codes and errors from self-calibration algorithm block of the same chips are as shown in Fig. 5. It can be seen that the codes in Fig. 4 for main ring and auxiliary ring oscillators are CTAT and PTAT, respectively. Even with certain process variation between chips, these variations have been eliminated by the self-calibration block. The calibrated output codes have a resolution of 0.5 °C. A micrograph of the fabricated chip is as shown in Fig.6.

IV. Conclusion

A self-calibrated low power delay line based temperature sensor is implemented and tested using a 65nm CMOS technology. Compared with conventional delay line temperature sensors, this self-calibrated design achieves a 2^N reduction in both power and energy consumption through the use of tab decoding along with a counter. The sensor only requires 0.02 nJ energy per conversion with a resolution of 0.5 °C and with errors less than ±2.0 °C over a temperature range from 20 to 80 °C. The sensing, decoding and timing blocks

TABLE I. SPECIFICATION COMPARED WITH PREVIOUS WORKS

Ref	Technology	Architecture	Area	Supply voltage	Power	Temperature Range	Resolution	Calibration Method	Accuracy	Energy per conversion
[9]	65nm	Bandgap	0.1 mm^2	1.2 V	10 µW	-70 ~125 ℃	0.03 ℃	Two-point	0.2 ℃	4.5 µJ
[2]	0.22µm	Delay line	N/A	2.5 V	175 µW	0 ~ 100 ℃	0.133 ℃	One-point	±0.7 ℃	175 nJ
[6]	0.13µm	Delay line	0.12 mm^2	1.2 V	1.2 mW	0 ~ 100 ℃	0.66 ℃	One-point	±2.3 ℃	0.24 µJ
[8]	65nm	Delay line	0.01 mm^2	1.0V	150 µW	0 ~ 60 ℃	0.139 ℃	Auto-calibration	±5.1 ℃	15 nJ
This work	65nm	Ring oscillator	0.002 mm^2	1.0V	60 µW	20 ~80 ℃	0.5 ℃	Self-calibration	±2 ℃	0.02 nJ

occupy an active die area of 0.002 mm^2. As indicated in Table I, the energy and active die area specifications are smaller than those reported in previous works. The proposed design can be fully synthesized using an automated place and route approach and can be easily ported to future CMOS technologies.

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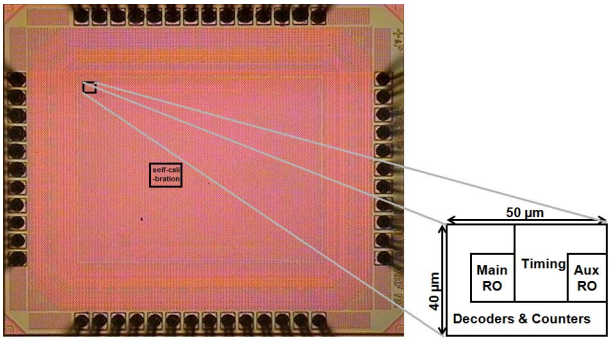

Figure 6. Micrograph of the fabricated temperature sensor. Die size is 1.5×1.3 mm^2, active area of the temperature sensor is 50×40 μm^2. This chip was implemented using TSMC's 65nm technology.

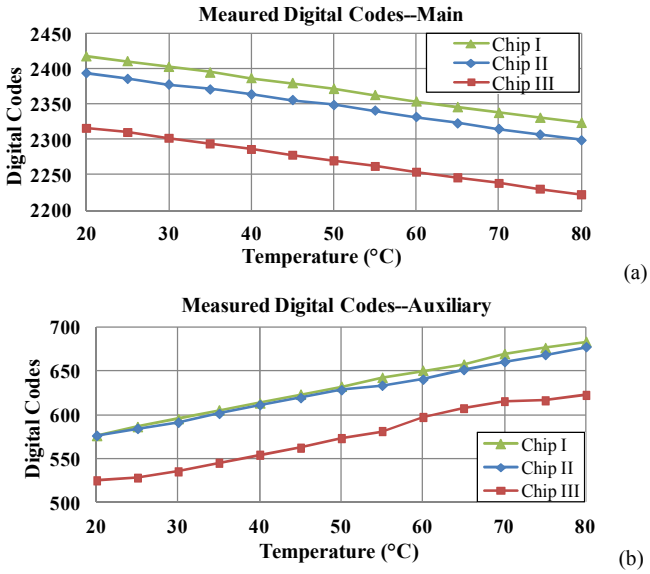

Figure 4. The measured un-calibrated digital codes from (a) the main and (b) the auxiliary ring oscillators, respectively.

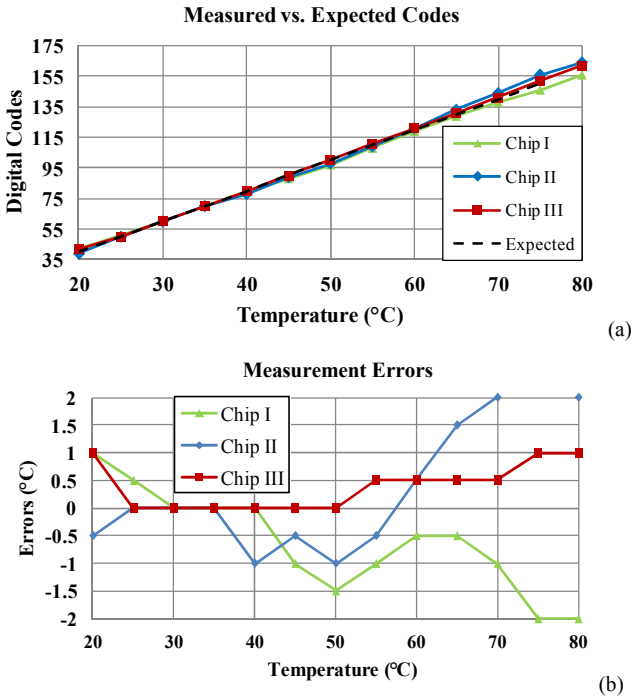

Figure 5. Measurement results from the self-calibration block.(a) measured versus expected codes, (b) measured temperature errors.