Current Balancing Control for Parallel Connected IGBTs Using Programmable Gate Driver Output Resistance

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***Abstract*— A gate driver IC with programmable output resistance (R_{out}) capable of performing current balancing for parallel connected IGBTs is presented in this paper. This novel method is to dynamically adjust the gate driver R_{out} to minimize the difference in the turn-on/off delay times between parallel connected IGBTs. The programmable gate driver R_{out} is implemented using a segmented output stage technique. This gate driver IC is designed and fabricated using TSMC's 0.18μm BCD Gen-2 process. Experimental results are obtained by measuring the current distribution between two parallel connected IGBTs (600V, 90A). These results indicate an improvement in average current imbalance of 89% and 98% for the turn-on and off periods, respectively.**

I. INTRODUCTION

In high power applications, switching devices such as IGBTs must often be connected in parallel to achieve a higher current rating. However, current is not shared equally between parallel connected IGBTs because of stray inductance, variations in device characteristic and asymmetric PCB layout. This leads to current imbalance between the IGBTs which necessitate de-rating of the devices. Unfortunately, de-rating leads to an increase in cost, size and complexity of the overall power electronics system. To minimize the current imbalance, manufacturers often pre-select or sort the IGBTs and gate drive units with similar performance. Despite these efforts, the maximum power rating for each IGBT module must still be reduced [1].

Current balancing methods for parallel connected IGBT modules have been reported by many publications. In [2], a resistor is inserted between each gate terminals. A current balancing controller varies di_C/dt and the gate voltage of the IGBTs. In [3-5], the current of each IGBT is monitored and controlled by an active gate controller by shifting the rising and falling edge of each gate signal (turn on/off timing of the IGBT), and adjusting gate voltage. In [6] and [7], the influence of various operating parameters on the IGBT switching behavior was investigated by simulation and experimental measurement. Their studies showed that delaying the gate signals has the strongest influence on current imbalance during switching and that the current imbalance can be compensated by controlling the delay time. A current balancing method for parallel connected IGBTs has been reported in our previous work [8] where the current balancing during the switching periods is achieved by dynamically adjusting the external gate resistance.

This paper proposes a new current balancing method that can be easily integrated and managed by a digitally controlled system. The proposed method is implemented with programmable gate driver circuits where their output resistance, R_{out} can be varied using a segmented output stage technique. Current imbalance during each switching period can be compensated by controlling the time delay of the IGBT's collector current pulse by changing the gate driver R_{out} dynamically. The functionality and performance of the proposed technique is experimentally verified by examining the behavior of parallel connected IGBTs rated at 600V and 90A.

This paper is organized as follows. The design, characteristics and theory of operation for the gate driver IC are discussed in Section II. The experimental test setup is described in Section III. Experimental results are presented in Section IV. Conclusions are provided in Section V.

II. GATE DRIVER IC WITH PROGRAMMABLE R_{OUT}

A. Gate Driver IC design

The circuit topology of the proposed gate driver IC is as shown in Fig. 1. The gate driver IC is composed of a digital control logic circuit and a segmented output stage [9], which is consisted of nine identical output segments connected in parallel as the high side switches and another nine identical output segments connected in parallel as the low side switches. Each segment can be individually enabled or disabled on-the-fly by the enable signals ($En_{HS}<n>$ or

En_{LS}<n>), which are generated in the digital control logic circuit by decoding an external 4-bit control signal (*Cbit<4:0>*). When a segment is disabled, the segment provides no current conduction path. A disabled segment therefore increases the overall R_{out} of the gate driver.

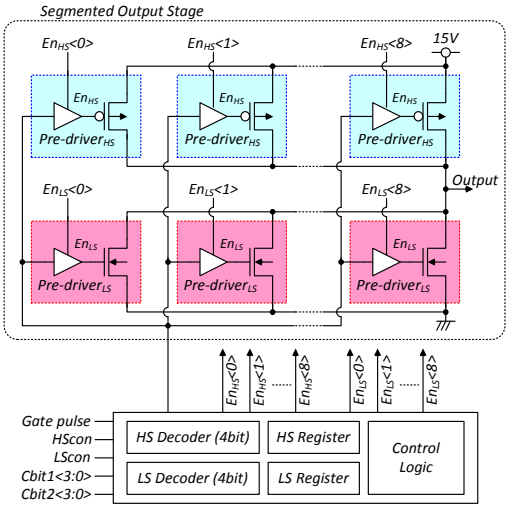


Figure 1. Topology of the proposed gate driver IC.

B. *Programmable gate driver R_{out}*

The gate driver IC is designed and fabricated using TSMC's 0.18µm BCD Gen-2 process. Chip area of the driver IC is 750µm × 520µm as shown in Fig. 2.

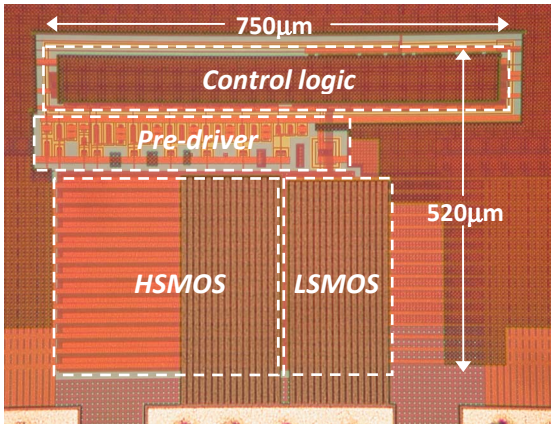


Figure 2. Micrograph of the proposed gate driver IC.

The measured output resistances for pull-up (High Side switches) and pull-down (Low Side switches) operation as a function of the control bits, *Cbit* are as shown in Fig. 3. R_{out} can be varied linearly between 2.5Ω and 80Ω. This feature makes it possible to control the switching behavior of IGBT during turn on period and during turn off period, individually.

Fig. 4 shows the input and output waveforms of the proposed gate driver IC with a capacitive load (C_{load} = 8 nF). They confirm that the R_{out} can be changed dynamically within the switching period and the time period that the R_{out} is changed can be controlled by the external control pulse (HS_{con} and LS_{con}).

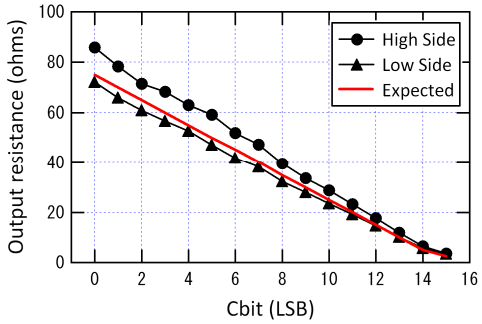


Figure 3. Measured and expected R_{out} of the gate driver IC.

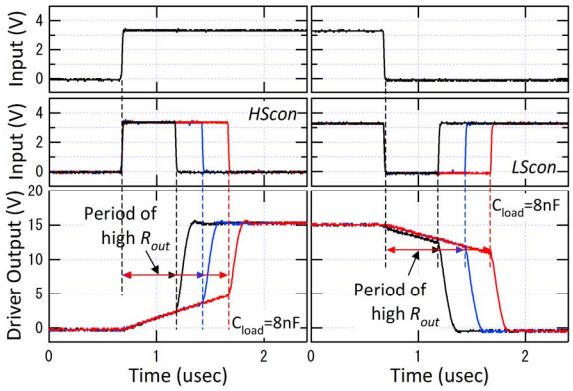


Figure 4. Input and output waveforms of the gate driver IC (C_{load} = 8 nF).

C. *Principle of Operation*

To achieve current balancing during switching, the turn on delay time (t_{d_on}) and the turn off delay time (t_{d_off}) must be controlled without lowering di_C/dt. In addition, the charge /discharge currents of the gate-collector capacitance (C_{GC}) supplied by the gate driver IC must not be limited while the collector-emitter voltage (V_{CE}) changes [8]. By changing R_{out} according to the timing diagram in Fig. 5 and adjusting both T_{con_on} and T_{con_off} appropriately according to the R_{out} value, t_{d_on} and t_{d_off} can be controlled without lowering di_C/dt and without limiting the charge/discharge current for C_{GC}.

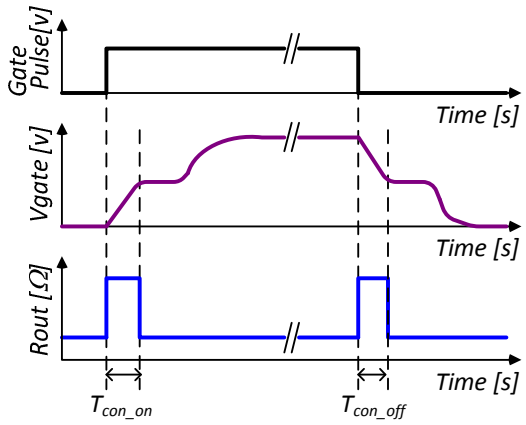


Figure 5. Timing diagram of the control signals for R_{out}.

III. Experimental Test Setup

In order to validate the current balancing technique with the programmable gate driver R_{out}, a double pulse test was conducted using a simple chopper circuit with two parallel connected IGBTs rated at 600V and 90A as shown in Fig. 6. Two fabricated gate driver ICs were incorporated into the chopper circuit to drive the parallel connected IGBTs, individually. The collector current of each IGBT is sensed using a sense IGBT in order to prevent any additional disturbance. The sensed current is converted to a voltage signal (V_{s1}, V_{s2}) via the sense resistor ($R_{sense1} = R_{sense2} = 50\Omega$). The current sense voltages, V_{s1} and V_{s2} are probed using an *Agilent Technologies MSO-X 3024A* mixed signal oscilloscope. All current waveforms in this paper are represented by the current sense voltage V_{s1} and V_{s2}. The gating signals and the dynamic R_{out} control signals (HS_{con} and LS_{con}) are generated using an *Altera Max II CPLD*.

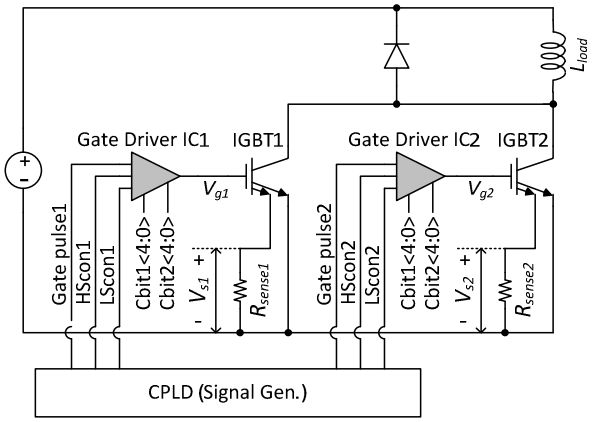


Figure 6. Test setup for current balancing experiment with the proposed gate driver ICs.

IV. Experimental Results

A. Switching Behavior for Individual IGBTs with Programmable Gate Driver R_{out}

The double pulse test was conducted with one gate driver IC disabled to measure the switching behavior for individual IGBTs. The switching behaviors with and without dynamic R_{out} control were measured with increasing gate driver R_{out} using *Cbit<4:0>* during turn on and turn off periods. Voltage waveforms for the input pulses of the gate driver IC (*Gate pulse* and HS_{con}/LS_{con}), gate node of IGBTs (V_g) and current sense node (V_s), with and without dynamic R_{out} control, during turn on and turn off periods are as plotted in Fig. 7 and Fig. 8, respectively. These behaviors confirm that t_{d_on} and t_{d_off} can be increased without lowering di_C/dt when the R_{out} is changed dynamically according to the timing diagram in Fig. 5. Variation in t_{d_on}, t_{d_off} and di_C/dt can be observed as R_{out} is changed. Furthermore, when R_{out} is changed dynamically according to the timing diagram in Fig. 5, R_{out} can be returned to the initial value just before the collector current is turned on or off and V_{CE} begins to change. Therefore, charge/discharge current of C_{GC} is not limited by increased R_{out} while V_{CE} changes.

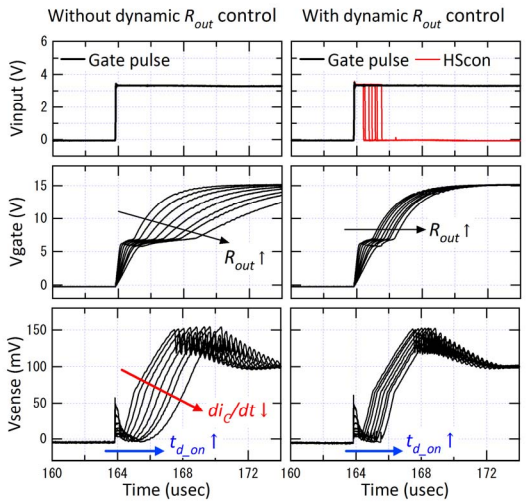


Figure 7. Switching behavior for individual IGBTs during turn on period.

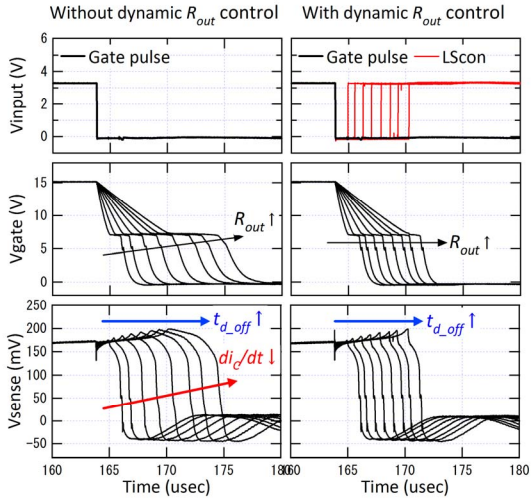
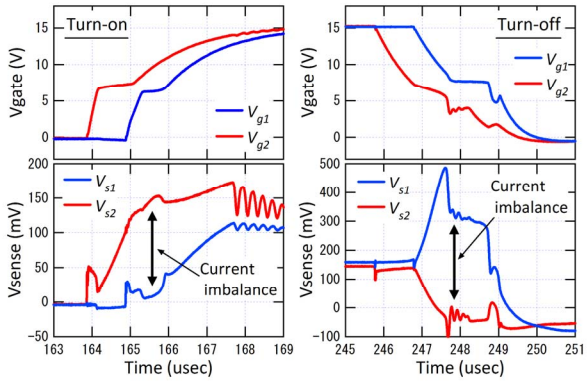


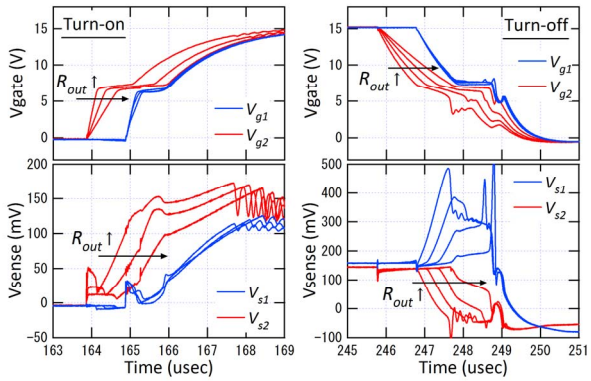
Figure 8. Switching behavior for individual IGBTs during turn off period.

B. Curent Balancing for Parallel Connected IGBTs

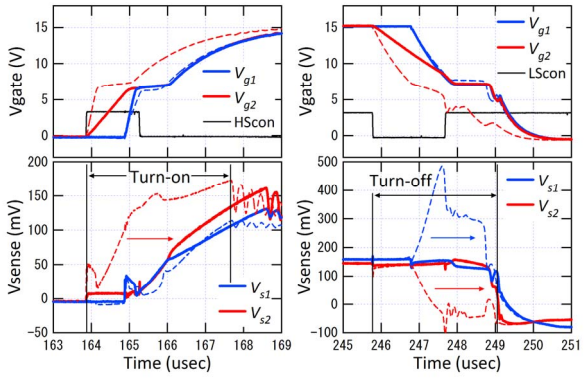
Fig. 9 shows the turn-on and turn-off waveforms at the gate node (V_{g1} and V_{g2}) and current sense node (V_{s1} and V_{s2}) for the parallel connected IGBTs. As shown in Fig. 9 (a), IGBT2 turns on and turns off earlier than IGBT1 because of the difference in t_{d_on} and t_{d_off}. Therefore, the total current is concentrated in IGBT2 during the turn-on period and is concentrated in IGBT1 during the turn-off period. As a result, without the dynamic R_{out} control, a significant current imbalance between IGBT1 and IGBT2 has been observed. By applying the dynamic R_{out} control and adjusting R_{out} and T_{con_on} and T_{con_off} of the gate driver IC2, t_{d_on} and t_{d_off} for IGBT2 are shifted and the large current imbalance between IGBT1 and IGBT2 is suppressed as shown in Fig. 9 (b). Finally, the current imbalance during turn-on and turn-off periods are minimized by optimizing R_{out} and T_{con_on} and T_{con_off} of the gate driver IC2 via *Cbit*, HS_{con} and LS_{con} as shown in Fig. 9 (c).



(a) Without dynamic R_{out} control



(b) With dynamic R_{out} control



(c) With dynamic R_{out} control (optimized R_{out}, T_{con_on} and T_{con_off})

Figure 9. Turn-on and turn-off waveforms at the gate node and current sense node for the parallel connected IGBTs.

The reductions in current imbalance during turn-on and turn-off periods as shown in Fig. 9 (c) are summarized in Table I. This data indicates an improvement of up to 77% and 93% in the maximum current imbalance and an improvement of up to 89% and 98% in the imbalance of the averaged current can be achieved.

TABLE I. IMPROVEMENT IN THE CURRENT IMBALANCE

		Without dynamic R_{out} control	With dynamic R_{out} control
Maximum current imbalance	T_{on}	Δ28.85 (A)	Δ6.52 (A)
	T_{off}	Δ168.48 (A)	Δ11.67 (A)
Imbalance of the averaged current	T_{on}	Δ18.64 (A)	Δ2.15 (A)
	T_{off}	Δ59.95 (A)	Δ0.99 (A)

V. CONCLUSIONS

A method for current balancing in parallel connected IGBT using the programmable gate driver R_{out} has been presented. The variation in R_{out} is accomplished using segmented output stage technique. Current balancing during the switching periods can be achieved by changing the gate driver R_{out} dynamically without high frequency digital logic or complicated time-delay circuitry. The experimental results show significant improvement in current balancing. This technique is simple and do not require extra die area and is suitable for digitally controlled system.

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