A Segmented Gate Driver IC for the Reduction of IGBT Collector Current Over-Shoot at Turn-on

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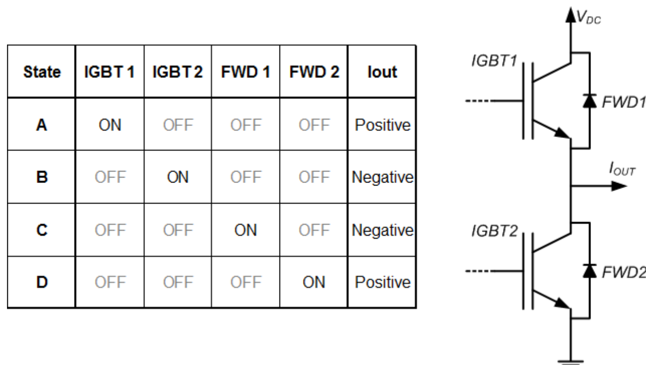
Abstract— **In this paper, a segmented IGBT gate driver IC for mitigating IGBT turn-on I_C over-shoot is presented. The proposed IC is fabricated using TSMC's 0.18 µm BCD Gen-2 process. Unlike existing I_C over-shoot reduction techniques, the proposed technique does not require significant additional external components or an increase in turn-on energy. During turn-on, the gate driver is controlled such that (dV_{GE}/dt) is kept low as current is transferred from the FWD to the IGBT and kept high at all other times. The ideal timing of (dV_{GE}/dt) transitions could vary between IGBT devices, age, temperature, etc. A feedback system is used to correct for these variances. A 37% reduction in I_C overshoot is achieved while maintaining the same E_{ON}. A 54% reduction in E_{ON} is achieved for the same I_C overshoot. Finally, a 15.5 dBm reduction in CEMI is observed when compared to operation with a constant R_{OUT} and similar E_{ON}.**

I. Introduction

In modern high voltage and high current power systems, simple and compact inverters are often constructed using Insulated Gate Bipolar Transistors (IGBT). As shown in Figure 1, an inverter is formed by connecting two IGBTs between a DC power supply line and ground. As the IGBT switches exhibit a unidirectional current flow, two Free Wheeling Diodes (FWD) must be added in order to allow for reverse current flow.

Figure 1 also summarizes the four possible states an IGBT inverter can exist in. By alternating between these states, the output current of the inverter, I_{OUT}, can be controlled.



State	IGBT 1	IGBT 2	FWD 1	FWD 2	Iout
A	ON	OFF	OFF	OFF	Positive
B	OFF	ON	OFF	OFF	Negative
C	OFF	OFF	ON	OFF	Negative
D	OFF	OFF	OFF	ON	Positive

Figure 1. IGBT inverter topology and operating states.

During transitions D→A and C→B, current is transferred from a FWD to an IGBT. This current transfer occurs as the FWD turns off while the IGBT turns on and is thus referred to as "IGBT turn-on". During IGBT turn-on, an abrupt increase in collector current (I_C) and even an I_C over-shoot will often occur [1]. Over-shoot in I_C can cause significant conducted EMI and reduce the lifetime of the IGBT [2]. A common solution to this problem is to reduce the rate at which the IGBT gate is charged during turn-on (dV_{GE}/dt) [1]. A reduction in (dV_{GE}/dt) is often achieved by inserting a resistor between the gate driver and the IGBT [1]. However, this approach also increases the IGBT turn-on time and subsequently the turn-on energy (E_{ON}) [1], reducing the overall power efficiency of the system.

In this paper, a segmented gate driver (similar to the MOSFET gate driver of [3]) is presented such that the output resistance of the gate driver (R_{OUT}) can be controlled digitally. An example of a segmented gate driver topology is as shown in Figure 2. Controlling R_{OUT} allows the rate of gate charging (dV_{GE}/dt) for the IGBT to be changed. Furthermore, multiple changes in R_{OUT} during a single turn-on transition are possible. By appropriately adjusting R_{OUT} in real time, a reduction in I_C overshoot can be achieved with little increase in E_{ON}.

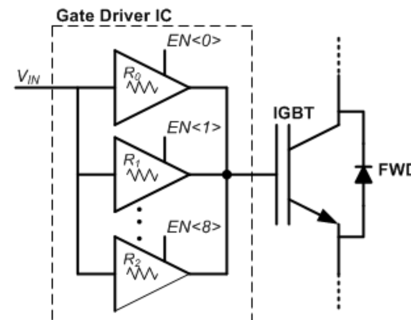


Figure 2. Proposed segmented gate driver IC.

Section II describes the physical design and operation of the gate driver IC. The experimental test setup is discussed in Section III. Experimental results for both I_C overshoot and conducted EMI are presented in Section IV. Finally, conclusions and future work are discussed in Section V.

II. PROPOSED TECHNIQUE

A. Gate Driver Design

The proposed gate driver IC of Figure 2 was fabricated in TSMC's 0.18 µm BCD Gen-2 process. A die photo of the resulting IC can be found in Figure 3. The gate driver IC is composed of 9 segments. The output resistance of each segment for both pull-up and pull-down is as listed in Table 1. A disabled segment presents the output with a high impedance state. Thus, when a segment becomes disabled, a charging/discharging path is removed and the output resistance of the gate driver increases. The IC was designed such that by enabling or disabling various segments, output resistances from 5 Ω to 150 Ω can be achieved in increments of 5 Ω.

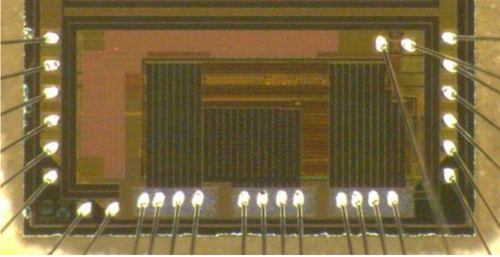


Figure 3. IC die photo (Area: 1mm × 2mm).

The segments are designed so as to maximize the ease of achieving the proposed technique. In particular, the segments are designed to exhibit minimal input to output propagation delay. Additionally, the propagation delay of each segment is matched. By achieving both of these goals, the output resistance of the gate driver can be quickly and consistently changed.

Table 1: Gate Driver Output Resistance

		Measured [Ω]	
Segment	**Designed [Ω]**	***Pull Up***	***Pull Down***
0	5	6.46	5.38
1	10	11.9	9.68
2	30	33.7	27.5
3	55	63.0	50.8
4	60	68.3	54.2
5	65	71.5	57.8
6	70	78.4	62.1
7	75	85.8	67.3
8	150	183	134

Each segment was built using the general structure as shown in Figure 4. The topology uses two cross-coupled inverter chains and an output stage composed of a single NMOS and a single PMOS. The inverter chain topology, a voltage driven approach, was selected in order to minimize propagation delay. An ancillary benefit to using voltage mode pre-drivers is the reduction of static power loss in the gate driver. In order to set the output resistance of a segment, the output NMOS and PMOS are appropriately sized. Furthermore, the delay from input to output was equalized between segments by independently adjusting the inverter chain taper for each segment.

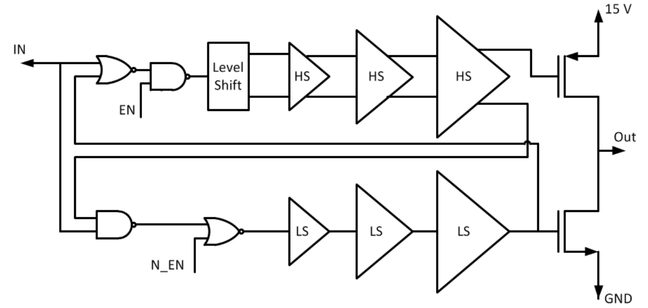


Figure 4. Gate driver segment topology.

In order to construct the voltage driven pre-driver topology discussed above, special attention must be given to the design of the high side (HS) inverters and the level shifter. This attention is required in order to avoid exceeding the V_{GS} breakdown voltage of 5 V. In this design, the HS buffers and the level shifter were constructed using the circuit topologies as shown in Figure 5.

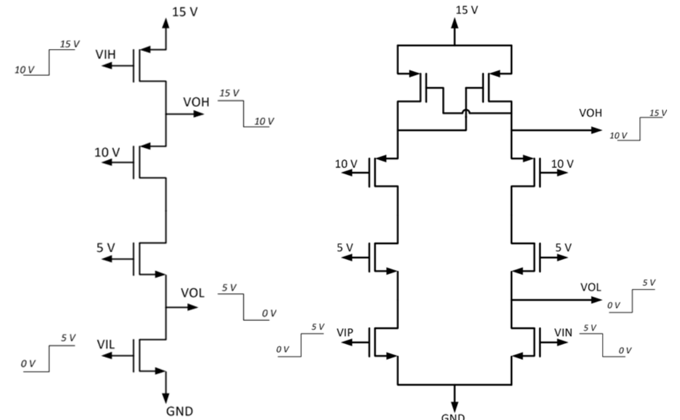


Figure 5. Segment sub-circuit designs (Left: HS Inverter, Right: Level Shifter).

B. Theory of Operation

During turn-on, as the gate voltage of the IGBT reaches the Miller plateau, V_{CE} begins to decrease and I_C begins to rise. The magnitude of I_C over-shoot is proportional to the value of (dV_{GE}/dt) as the Miller plateau is reached [1], at point T_{FALL} in Fig. 6. Thus, in order to eliminate I_C overshoot without significantly increasing E_{ON}, (dV_{GE}/dt) is kept high at all points, except near point T_{FALL}, as shown in Figure 6.

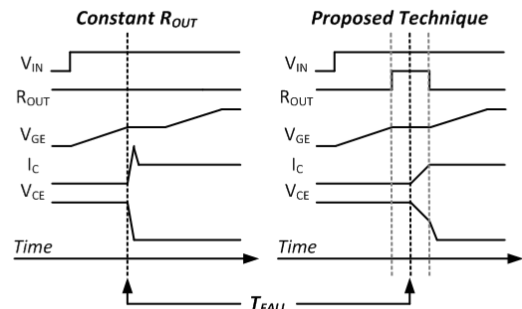


Figure 6. Proposed gate driver operation.

Similar methods include the modulation of (dV_{GE}/dt) by controlling the gate driver supply voltage [2][4], analog control of the gate driver output current [5] and the addition of switched capacitors in parallel with the gate of the IGBT [6]. However, all of these existing approaches require either the addition of complex circuitry, an increase in gate driver die size or the addition of several external components; problems which are eliminated with the proposed segmented gate driver IC.

III. Experimental Test Setup

A schematic of the test bench for the gate driver IC can be found in Figure 7. Two gate driver ICs are used to drive two IGBT switches arranged in an inverter topology. The IGBTs are rated at 600 V and 30 A. In order to measure the point when T_{FALL} occurs, V_{OUT} is measured using a HV diode and a resistor. By measuring the timing of T_{FALL}, the R_{OUT} transitions can be continually adjusted in order to ensure that T_{FALL} occurs when R_{OUT} is high, ensuring a low (dV_{GE}/dt) during T_{FALL}. An Altera Cyclone II FPGA was used to generate the required control signals for the gate drivers. A summary of the system specifications for the test bench can be found in Table 2. Due to equipment limitations, different current and voltage levels were used for the I_C overshoot tests and the conducted EMI tests. In order to verify the effectiveness of the proposed technique, I_C for the high side IGBT (HS IGBT) was observed during IGBT-turn on. I_C was determined by measuring I_{SUPPLY} using a current probe. Additionally, the V_{CE} and V_{GE} voltages of the HS IGBT were measured during IGBT turn-on. Finally, conducted EMI measurements were performed by probing the supply voltage (V_G) using a spectrum analyzer.

Figure 7. Gate driver test bench schematic.

Table 2: Gate Driver Test Bench System Specifications

Parameter	I_C/E_{ON}	CEMI
V_G	200 V	20 V
I_L *(At turn on)*	4 A	16 mA
V_{DD}	15 V	15 V
Switching Frequency	20 kHz	20 kHz

IV. Experimental Results

A. Turn on Energy and Current Overshoot

In order to verify the proposed technique, the voltage and current waveforms for the high side IGBT were measured during turn-on for several conditions. Figure 8 shows the switching waveforms for a constant R_{OUT} of 6.46 Ω. Figure 9 shows the same waveforms but for a constant R_{OUT} of 85.8Ω. Finally, Figure 10 shows the switching waveforms for the proposed technique. It can be clearly seen from Figures 8 and 9 that an increased R_{OUT} produces less I_C overshoot and lowers the amount of ringing. However, these benefits come at the expense of turn-on time, which is significantly increased in Figure 9.

Figure 8. V_{GE}, V_{CE} and I_C for constant R_{OUT} of 6.46 Ω [V_{CE}: 50V/div, V_{GE}: 5 V/div, I_C: 2A/div].

Figure 9. V_{GE}, V_{CE} and I_C for constant R_{OUT} of 85.8 Ω [V_{CE}: 50V/div, V_{GE}: 5 V/div, I_C: 2A/div].

Figure 10. HS IGBT V_{GE}, V_{CE} and I_C for the proposed technique with R_{OUT} switched between 6.46 Ω and 85.8 Ω [V_{CE}: 50V/div, V_{GE}: 5 V/div, I_C: 2A/div].

Figure 10 shows that the proposed technique is capable of reducing I_C overshoot and ringing while reducing the turn-on time of the IGBT. Finally, Figure 11 compares the proposed technique to many different constant R_{OUT} situations by plotting E_{ON} against the level of I_C overshoot. E_{ON} was calculated by multiplying V_{CE} by I_C and integrating over the entire turn-on period.

The constant R_{OUT} operation exhibits an inverse relation between E_{ON} and I_C overshoot. This result shows that as R_{OUT} increases, turn-on time increases, and subsequently E_{ON} increases. However, the proposed technique is capable of breaking this relationship. A 37% reduction in I_C overshoot is achieved while maintaining the same E_{ON}. Additionally, a 54% reduction in E_{ON} is achieved for the same I_C overshoot.

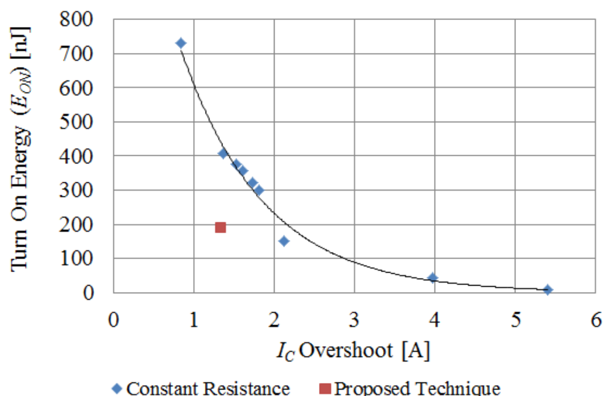


Figure 11. E_{ON} vs I_C overshoot.

B. Conducted EMI Improvement

In order to investigate the impact of the proposed technique on conducted EMI (CEMI), tests for several values of R_{OUT} and the proposed technique were performed. Figure 12 shows the measured CEMI spectrum for a constant R_{OUT} of 9.68 Ω. Figure 13 shows the measured CEMI spectrum for the proposed technique. For the CEMI measurements of Figures 12 and 13, E_{ON} was approximately equal, 9 nJ and 8 nJ, respectively. Comparing Figures 12 and 13, it can be see that the proposed technique offers a reduction in peak CEMI of 15.5 dBm above 10 MHz.

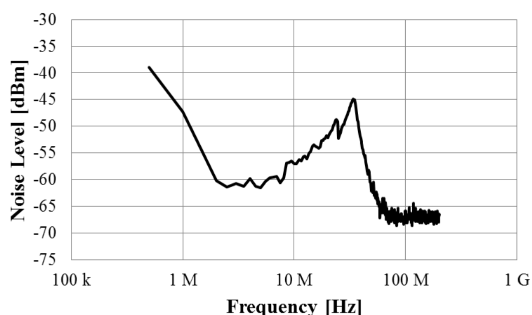


Figure 12. CEMI measurement for a constant R_{OUT} of 9.68 Ω.

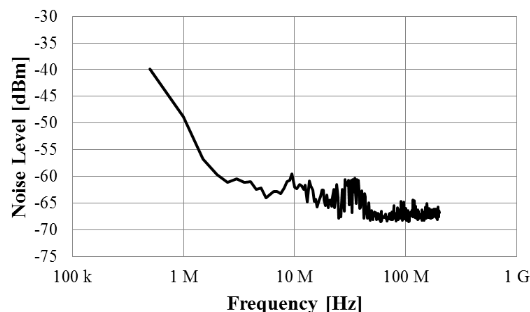


Figure 13. CEMI measurement for the proposed technique.

V. Conclusions and Future Work

The proposed technique is capable of reducing IGBT turn-on I_C overshoot without a corresponding increase in E_{ON}. For a similar E_{ON}, the proposed technique is capable of reducing the I_C overshoot by 37 %. For a similar I_C overshoot, the proposed technique is capable of reducing E_{ON} by 54 %. Additionally, the proposed technique was observed to reduce CEMI by 15.5 dBm when compared to operation with a constant R_{OUT} exhibiting a similar E_{ON}. Finally, the observed improvements do not incur a significant increase in extra discrete components. Moving forward, the authors intend to fabricate the required digital control logic and sensing circuitry on the same die as the gate driver. This design change will fully integrate the proposed technique and allow the entire process to be hidden from the power system designer.

Acknowledgements

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