Design of a Rugged 60V VDMOS Transistor

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Abstract

Vertical Double Diffused MOSFET (VDMOS) is an established technology for high-current power switching applications such as automotive circuits. The most serious failure mode is destructive damage during inductive switching, resulting from avalanche breakdown of the forward blocking junction in the presence of high current flow. Improving the ruggedness of the device is achieved by enhancing its ability to absorb inductive energy under avalanche conditions. The purpose of this paper is to explore the possibility of improving the ruggedness of VDMOS through TCAD simulations. A p^+-strip buried underneath n^+-source is proposed to suppress the turn-on of the parasitic bipolar transistor. VDMOS transistors with this design modification is expected to have higher ruggedness while maintained its superior figure-of-merit.

Keywords: power MOSFET, VDMOS, snap-back behaviour, UIS, avalanche breakdown, ruggedness, TCAD

INTRODUCTION

Growing demand in efficient power MOSFET switches has prompted the need for robust VDMOS (Vertical Double Diffused MOS) transistors with ultra-low power loss. In applications with higher frequency switching (e.g. >1 MHz), the gate drive loss becomes more significant. Therefore, the optimization of a low-loss (switching and conduction losses) power MOSFET requires a better tradeoff between on-state resistance and gate input capacitance [1, 2]. Moreover, the most serious failure mechanism is destructive damage for power VDMOS during inductive switching. This is commonly caused by avalanche breakdown of the forward blocking junction in the presence of high current flow [3, 4].

In this paper, the development of a 60V VDMOS technology that offers high ruggedness is presented. The reference VDMOS is based on an existing technology from Asahi Kasei Microsystems Co. Ltd. (AKM). A proposed enhancement to further improve the device ruggedness is confirmed via device and process simulations.

DEVICE STRUCTURE

The typical device structure of a generic *n*-VDMOS is as shown in Fig. 1. The cell layout is in hexagonal shape to maximize the ratio of device channel width to the chip area in order to maximize its figure-of-merit (FOM). This number is the product of device on-resistance (R_{on}) and gate charge (Q_g), and is widely used to evaluate the efficiency performance of power MOSFETs. The device structure is based on the double diffusion of the p-body and *n*+ source regions using the edge of the polysilicon as a masking boundary.

By using TCAD tools (ISE), the device fabrication process and device structure have been developed. The voltage handling capability is determined by the breakdown voltage of the *p*-body/*n*-epi layer junction and is strongly dependent on the thickness and the doping of the lower doped *n*-epi layer. Fig. 1 also shows the electric field distribution upon breakdown at 65 V. The device is optimized to have the highest electric field occur at the bottom of *p*-body/*n*-epi layer junction.

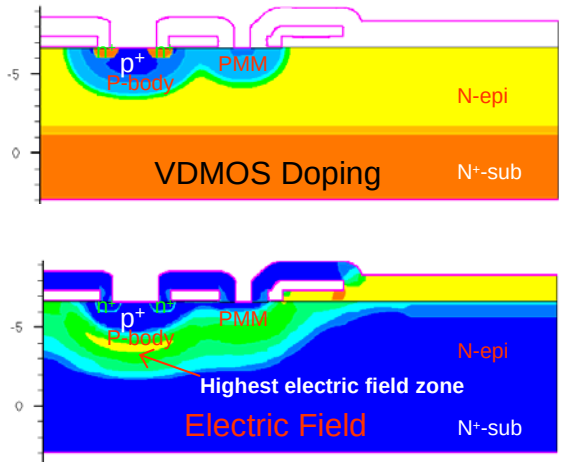

Fig. 1: The simulated *n*-VDMOS structure and its electric field distribution at a breakdown voltage of 65V.

VDMOS FABRICATION PROCESS

The reference VDMOS was based on a 0.5 µm process developed by AKM. The starting wafer is a <100> oriented, n^+-type wafer with nominal arsenic doping

concentration of 10^{19} cm^{-3}. At the beginning of the fabrication process, the wafers undergo epitaxial growth of an n^--layer with phosphorus doping concentration of 10^{16} cm^{-3}. Then, field oxidation is carried out to form a thick layer of oxide followed by active lithography and oxide etching to define the device area. After that, gate oxidation, poly-silicon deposition, doping anneal, gate lithography, and poly-etch forms gate pattern of hexagon-mesh. A self-aligned implantation of boron and anneal forms *p*-body, while a self-aligned implantation of arsenic and anneal forms n^+-source. The lateral diffusion difference of the *p*-body and n^+-source forms a controlled channel length along the *Si*-surface. The choice of doses is based on diffusion trials and extensive process and device simulations. A masked high dose boron implantation is carried out to form p^+-region in the p-body to enhance the body contact.

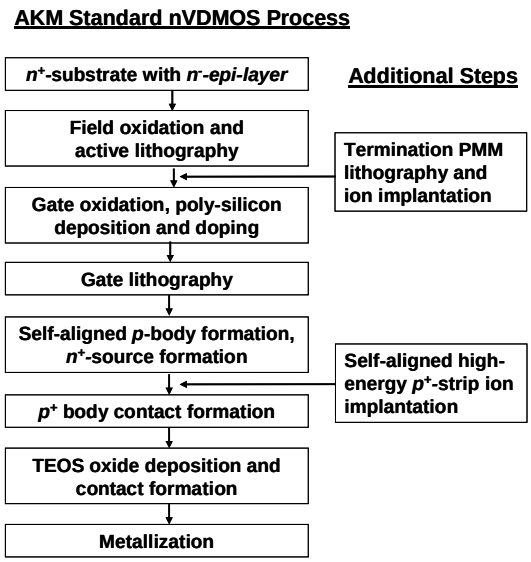

Fig. 2: AKM VDMOS process flow with additional steps to enhance device ruggedness

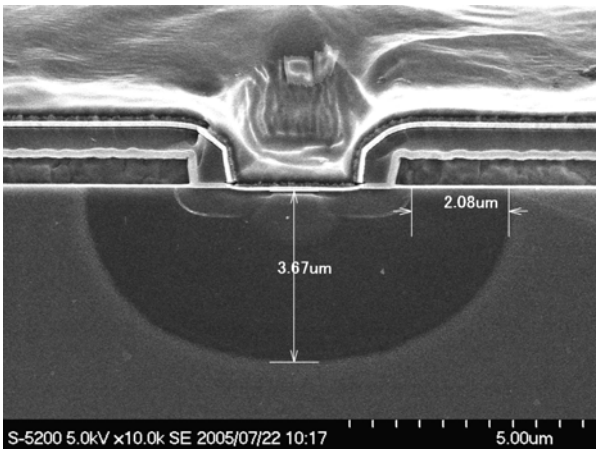

Fig. 3: SEM cross-sectional structure of a fabricated *n*-VDMOS

After that, a thick inter-level oxide deposition of TEOS is followed by contact lithography and oxide etching to form the contact window. Finally, metallization covers the chip surface and forms the butting source/body contacts for the VDMOS. By distributing metal contacts on the polysilicon gate around the edge of the chip, the device's gate resistance is minimized. Fig. 2 illustrates the general flow of this fabrication process, the proposed steps are added to improve the device ruggedness.

SEM cross sectional micrograph of the reference device is shown in Fig. 3. It has a channel length of about 2.0 µm and *p*-body/n^--epilayer junction depth of 3.67 µm. The device achieves a specific on-resistance of 1.2 mΩ·cm^2, breakdown voltage of 63 V, and an FOM of 1210 mΩ·nC.

DEVICE RUGGEDNESS ANALYSIS

In order to improve the device ruggedness, the ability to sustain an avalanche current during an unclamped inductive load switching event must be improved. At the same time, the turn-on of the parasitic drain-body-source *npn* BJT must be suppressed. ISE device simulation shows that the maximum electric field, in a conventional VDMOS, spreads across the *p*-body underneath the n^+ source region. As shown in Fig. 4, the avalanche breakdown initiated in this high electric field region could generate massive electron-hole pairs. From there, electrons are swept across the drain while holes flow through the *p*-body regions and the p^+ diffusion towards the source metal contact. The resistance in these *p*-regions will cause a potential drop beneath the n^+ diffusion. If this resistance is not small enough, the *pn*-junction may become forward biased.

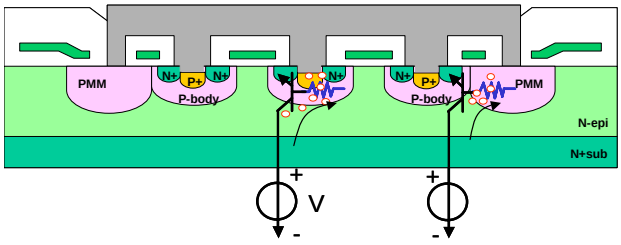

Fig.4: Schematic diagram of turning-on parasitic drain-body-source *npn* BJT in a VDMOS upon switching. Open circles represent holes, the paired electrons are not illustrated.

On the other hand, if defects are present in the silicon or if the device fabrication does not yield uniform characteristics across the entire transistor, avalanche multiplication will be most likely a local event. This could cause a high avalanche current density flowing beneath the source n^+ region and give rise to a potential drop sufficient to forward bias the *pn*-junction. All these factors could turn-on the parasitic *npn* bipolar transistor inherent in the VDMOS structure.

For the purpose of evaluating the device ruggedness, a UIS (unclamped inductive switching) test [5] in single shot mode is employed to quantify the ruggedness in the event of avalanche breakdown. In preliminary testing, the device in DPAK package achieves a UIS avalanche energy of 150 mJ which is almost at the same level as the commercially available IRFZ24N device. As the photo-emission analysis shown in Fig. 5, the device generates a large among of hot electrons at the periphery upon UIS avalanche breakdown. Due to the positive temperature coefficient associated with a forward biased *pn*-junction, current crowding will rapidly drive the device to a secondary breakdown and eventual destruction.

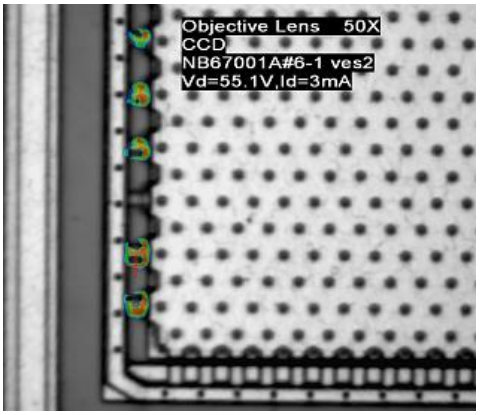

Fig. 5: Photo-emission analysis of an experimental device with breakdown occurring at the periphery, indicating possible parasitic *npn* turn-on during UIS testing.

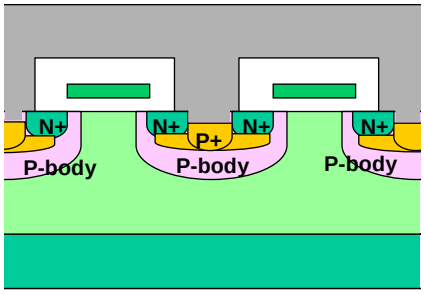

Fig. 6: Schematic cross section of a modified *n*-VDMOS with buried p^+-layer placed underneath the n^+ source

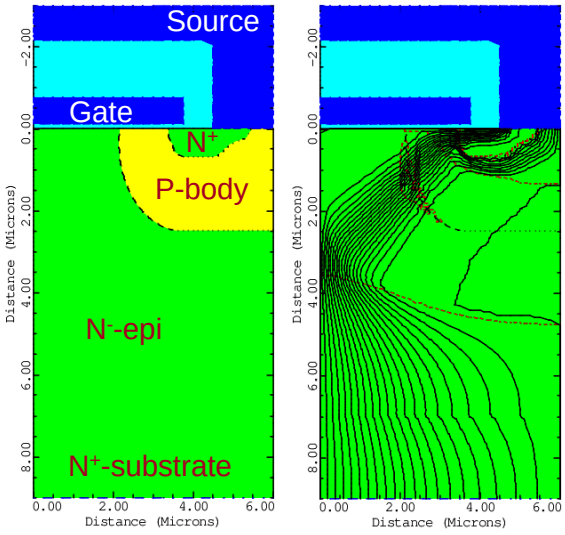

Fig. 7: Half structure of an n-VDMOS device and 5% flowlines upon snapback breakdown.

In order to reduce the possibility of activating the parasitic *npn*, we propose a unique source structure as illustrated in Fig. 6. In comparison to a conventional VDMOS, a strip of highly doped p^+-region is inserted at the n^+-source/*p*-body junction. This results in a lower drift resistance without increasing gate-drain capacitance and device on-resistance.

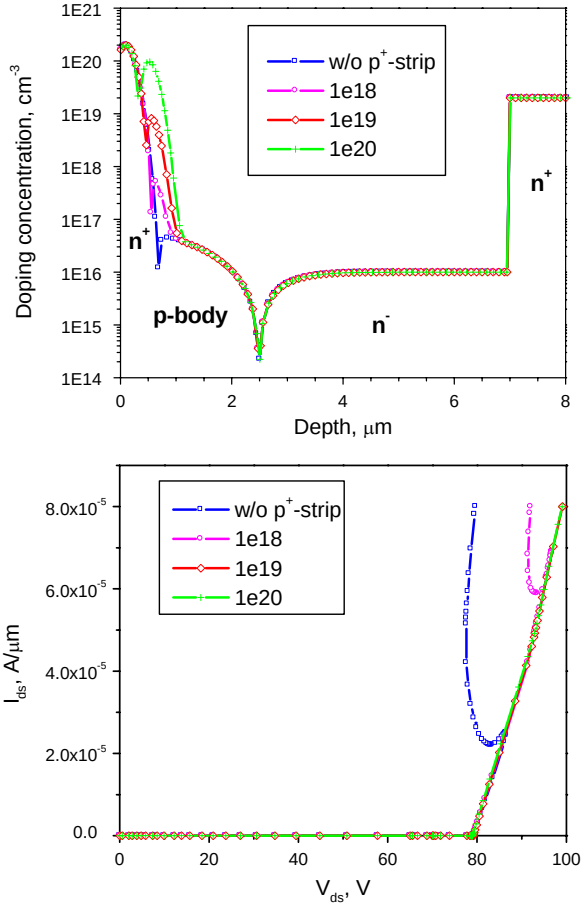

Fig.8: Improvement of drain current behaviour by introducing confined p^+-strip underneath n^+-source

To verify the effectiveness of this p^+-buried layer under the soure region, the tendency to show snapback breakdown behavior is evaluated. Fig. 7 shows the half structure of a MEDICI-simulated n-VDMOS device and its 5% flowlines

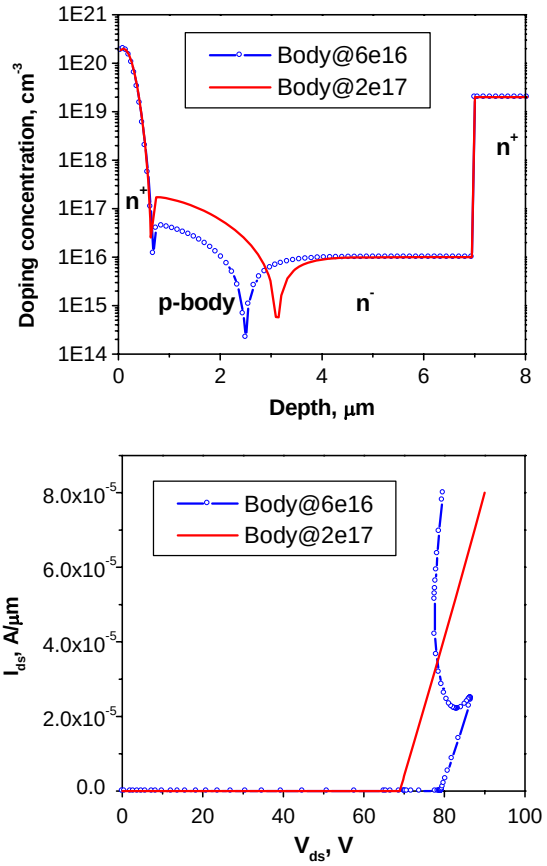

Fig.9: Improvement of drain current behaviour by increasing *p*-body peak concentration

upon snapback breakdown. Here, each current flowline represents 5% of the total current. It is clearly shown that the parasitic *npn* transistor is turned on. The lateral flowlines at the bottom of the n^+-source generates the body-to-source voltage that eventually turns on the transistor.

Fig. 8 gives the doping profiles of the simulated device with different doping concentration of p^+-strip, their corresponding I_{ds} *vs* V_{ds} curves are also illustrated in the same figure. With p^+-strip peak concentration increased to over 1×10^{19} cm^{-3}, the snapback behavior could be avoided. Simulation also confirmed that device threshold voltage and channel length remain the same.

In contrast, Fig. 9 shows the doping profiles of the reference device with different *p*-body doping concentration and their I_{ds}~V_{ds} curves. Increasing the *p*-body doping concentration from 6×10^{16} to 2×10^{17} cm^{-3} also can suppress the snapback behavior. However, this decreases the device breakdown voltage from 72 V to 65 V. The threshold voltage also increases from 3.1 V to 5.8 V while the channel length also increases from 1.36 μm to 1.76 μm. As a result, the device's on-resistance increases. Moreover, it also increases the drain-to-body capacitance (C_{gd}) which is the dominating factor in VDMOS to slow

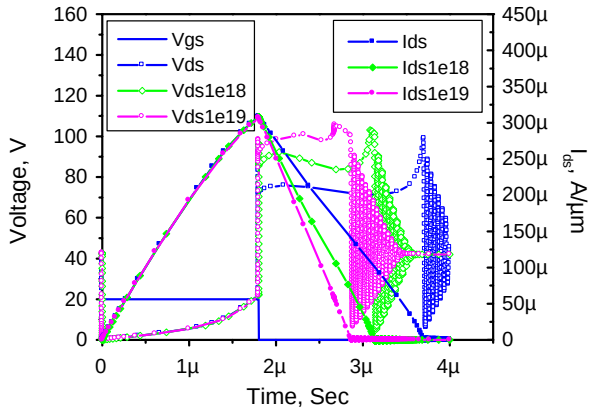

Fig.10: Waveform of devices with different p^+-strip peak concentrations during UIS switching. The oscillations indicate numerical instability at the end of the simulation.

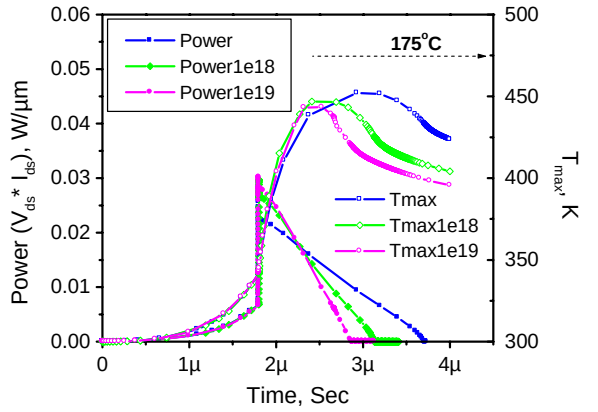

Fig.11: Transient of instantaneous power consumption and maximum lattice temperature during UIS switching of devices with different p^+-strip peak concentrations. Note the device is referred to be burned if T_{max} reaches 175°C.

down the device switching speed. Therefore, increasing the *p*-body doping concentration is not a good approach to improve the device ruggedness.

Since the potentially destructive DC snapback breakdown behavior can be triggered by the UIS event, it would be appropriate to simulate UIS characteristics. UIS simulations were also carried out using MEDICI. Fig. 10 shows the waveform generated during UIS switching. The instantaneous power and maximum lattice temperature (T_{max}) in the simulated device are also plotted in Fig. 11 along as a function of time. Under the same UIS switching condition, I_{ds} drops quicker with increasing p^+-strip peak concentration. As a result, the integrated energy dumped from inductor is less and the peak T_{max} is lower. The UIS ruggedness is improved by about 24% if a p^+-strip of 10^{19} cm^{-3} is introduced. Fig. 12 shows the lattice temperature contour when simulated devices reach their peak T_{max}. It is

clear that the device structure without the p^+-strip has vast number of hot spots which will eventually turn-on the parasitic *npn* transistor, leading to the destruction of the device.

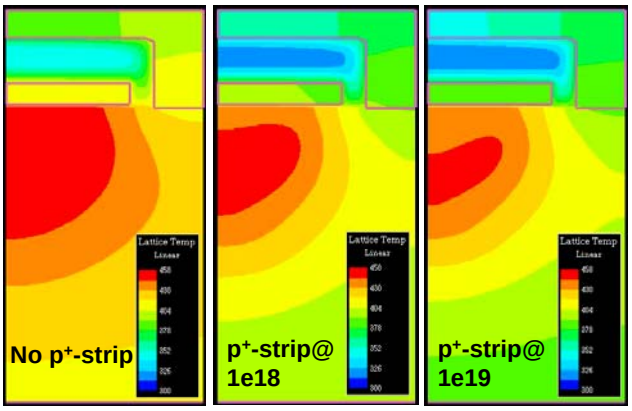

Fig.12: Temperature contours of devices with different p^+-strip peak concentrations when T_{max} reaches its peak during UIS simulation

CONCLUSIONS

A simple way to improve VDMOS ruggedness without introducing degrading factors to other performances has been presented. The new process only requires an additional thin-layer of highly doped p^+-strip underneath n^+ source / *p*-body junction. TCAD simulations proved its effectiveness in improving device ruggedness, an improvement of UIS ruggedness as high as 24% over the conventional device is expected.

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