A Low Power All-digital Self-calibrated Temperature Sensor using 65nm FPGAs

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***Abstract* — This paper presents an all-digital self-calibrated delay-line based temperature sensor. A continuous self-calibration technique is proposed to remove process variations and to generate direct digital representations of temperature. A power saving scheme using a hybrid counter/pulse position decoder is also introduced without any increase in area overhead. Four different architectures including traditional long and short delay-lines, and the proposed power saving hybrid sensor with long and short delay-lines are implemented on multiple 65nm Cyclone III FPGAs along with an on-chip continuous self-calibration circuit. The logic utilization for a single sensor is as small as 60 Logic Elements (LE) and its measured power consumption is as low as 2.9 µW, with errors less than ±1.6 ºC from 20 ºC to 75 ºC.**

I. INTRODUCTION

Digital temperature sensors are used in modern microprocessor to gather thermal information at critical locations, facilitating thermal management [1]. Due to the varying activities across different cores, it is necessary to position a large number of sensors on the same die. This further tightens the area and power requirements for the digital temperature sensors. As these sensors are surrounded by digital logic circuit, it is best that they can be designed to share the same power grid [1]. Accurate bandgap based temperature sensors occupy a large die area (typically > 0.1 mm^2) [2]. In contrast, digital delay-line based temperature sensors are low power, area efficient, synthesizable and well suited for the above applications.

Numerous all-digital delay-line based temperature sensors have been published previously [3]-[7]. However, none of them have automated self-calibration capability except [4], which has to rely on accurate simulation results. We have previously reported an effective all-digital temperature sensor with self-calibration implemented using FPGA [8]. This paper proposes an enhanced power saving architecture with continuous self-calibration capability. In addition, an accurate off-chip bandgap temperature sensor is used to further enhance the performance of all the on-chip digital temperature sensors. A block diagram of this configuration is as shown in Fig. 1. Experimental results from four different temperature sensor architectures implemented in 65nm FPGAs are used to verify the proposed method. The rest of this paper is organized as follows: Section II introduces the operating principle of the power saving method. The continuous self-calibration method is described in Section III. Experimental results are discussed in Section IV, followed by the conclusions in Section V.

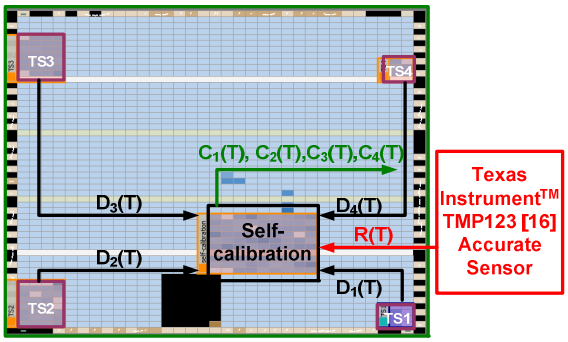

Figure 1. Placement of the proposed temperature sensors, showing their relative sizes. TS3 and TS4 are the proposed temperature sensors with short and long delay lines.

II. OPERATING PRINCIPLE AND DESIGN OPTIMZATION

A. *Power-saving method*

The propagation delay of a single inverter has a positive temperature coefficient, due to the negative temperature coefficient of the surface carrier mobility for electrons [3], [9]. The frequency of a delay-line based ring oscillator is inversely proportional to the propagation delay of the inverter and the length of the delay-line as shown in Fig. 2(a). A counter is used to count the number of pulses from the ring oscillator within a fixed gating time [7], [8] and generates the digital outputs that are proportional to temperature. In [3] and [5], an on-board crystal oscillator frequency (50 MHz) and a counter are used to form a time-to-digital converter (TDC). A high frequency is required to maintain an adequate TDC resolution, but at the expense of high power consumption. The ring oscillator based structure as shown in Fig. 2(a) is able to reduce the counter's power consumption by increasing the length of the delay-line (or decoder). HSpice simulation

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results using TSMC's 65nm CMOS technology validate this claim. The results are as shown in Fig. 3. A trade-off between area and power consumption can be clearly observed. The proposed method alleviates this problem by using a decoder along with the counter. As shown in Fig. 2, for a temperature sensor with M-bit resolution, the counter provides the (M□N) MSBs while the decoder captures the position where the input reset pulse stops within the ring oscillator and generates the remaining N LSBs. This method was originally proposed in [10] for the generation of DPWM signals and in [11] for time based analog-to-digital converter (ADC). The calculated total dynamic power and energy per conversion using the proposed power saving method are:

$$P_{dyn} = P_{dyn\_ringoscillator} + P_{dyn\_counter} = V_{DD} \cdot i_{ave} + V_{DD} \cdot i_{ave} \cdot \frac{C_{counter}}{C_{inverter}} \left(\sum_{x=0}^{M-N} \frac{1}{2^x} \right) \quad (1)$$

$$E = P_{dyn} \cdot \frac{1}{f_s} = \frac{D_{coarse}}{2^N} \cdot V_{DD}^2 \cdot \left(C_{inverter} + \frac{C_{counter}}{N_{stage}} \left(\sum_{x=0}^{M-N} \frac{1}{2^x} \right) \right) \quad (2)$$

Intuitively, the proposed method (1) can save power by using a counter with a lower number of bits.

B. *Reduction of digital outputs variations in time domain*

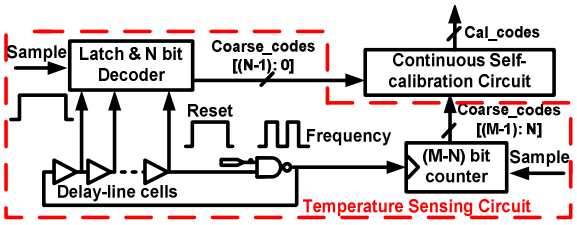
Outputs variations due to jittering are reported in delay-line based temperature sensors [6]. Jittering is mainly due to the flicker noise and white noise in the ring oscillator and the induced phase noise is inversely proportional to the length of the delay-line [12]. However, increasing the length of the delay-line will increase chip area. It has been demonstrated that jittering can be reduced by resetting the oscillator in shorter intervals [13]. Therefore, in the proposed work, the outputs are reset 8 times during the sampling period, as shown in Fig. 2(b). This technique can be considered as a form of averaging. The temperature errors as shown in Fig. 4 are obtained using 1250 samples from three different architectures with and without this averaging technique. Fig. 4 indicates that for all architectures, the measured errors decrease as the length of delay line increases. Also, the proposed averaging method can effectively reduce the measurement errors.

III. CONTINUOUS SELF-CALIBRATION

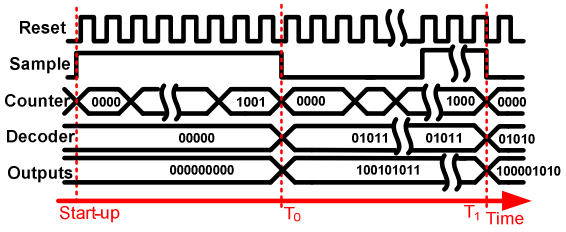
An earlier work proposed that the propagation delay of a logic inverter can be treated as the product of temperature-only-dependent component T^{α} and a process-only-dependent component $G(P)$: $D(T, P) = T^{\alpha} \cdot G(P)$ [6]. Dividing $D(T, P)$ by $D(T_C, P)$ (at a reference temperature), a normalized delay at T can be generated as:

$$D_{\text{norm}}(T) = D(T,P) / D(T_C,P) = (T / T_C)^{-\alpha} \quad (3)$$

where $D_{\text{norm}}(T)$ depends only on temperature (independent of process variations). Based on the above assumption, one-point calibration methods were performed by forcing all the sensing delay lines to have the same propagation delay at 50 ºC [5], [6]. However, neither of these two calibration procedures are automatic, as [6] requires switching between calibration and measurement modes while [5] needs an off-chip timing comparison circuit. In this work, a correction



(a) Architecture of the proposed design.



(b) Timing diagram when M = 9, N = 5.

Figure 2. Architecture and timing diagram of the proposed design.

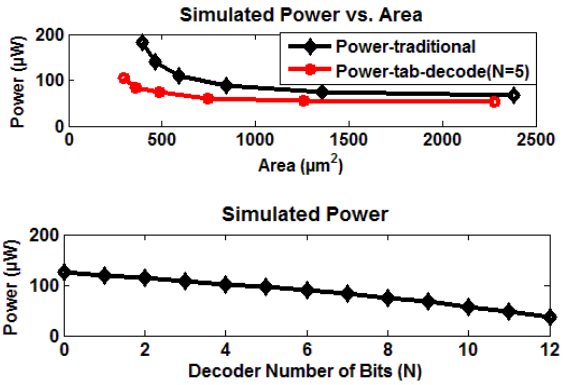


Figure 3. Simulated power is reduced as the number of bits in the decoder increases.

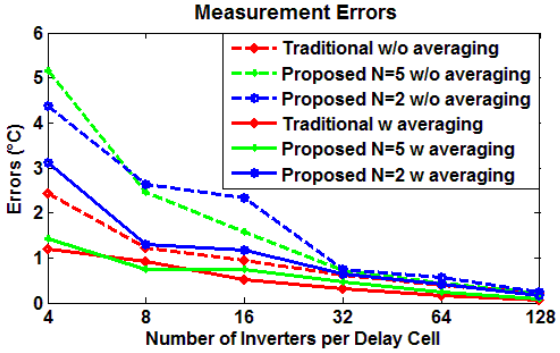


Figure 4. Errors caused by jittering are reduced by the proposed averaging method.

factor N_C is computed during start-up. This factor is used to multiply each sensor's digital outputs:

$$C(T_1) = D(T_1,P) \cdot N_C = C(T_C) \cdot D(T_1,P) / D(T_C,P) = C(T_C) \cdot (T / T_C)^{-\alpha} \quad (4)$$

$$N_C = C(T_C) / D(T_C,P) \text{ [8]}$$

where $C(T_1)$ and $C(T_C)$ stand for calibrated codes at any temperature T_1 and reference temperature, respectively. The proposed continuous self-calibration method was first

proposed in [8]. This calibration method not only removes process variations, but also calibrates one of the sensors against an accurate on-chip temperature reference to obtain chip-level gain and offset. This offset and gain are then applied to all the sensors on the same chip. A flow chart showing the continuous calibration process is as shown in Fig. 5. $H(T_X)$ is the final calibrated outputs. *GS* and *GR* are the gains (in K^{-1}) for the delay-line based sensors and the accurate reference sensor, respectively. *OFFSET* is the offset of the delay-line sensor. *DIFF* is a specified number for determining when to capture the second temperature point for continuous calibration. $R(T)$ stands for the accurate sensor digital outputs, $D(T)$ stands for the un-calibrated delay-line sensor outputs and $C(T)$ stands for the calibrated delay-line sensor outputs. The continuous self-calibration process operates as follows. At start-up, all sensors are assumed to be at the same temperature. A correction factor N_C is obtained from each sensor's digital outputs at startup temperature using (3) and is multiplied to each sensor's digital outputs, making all sensors' digital outputs to be the same at startup temperature. After the process variations are removed, the continuous calibration begins. Both the accurate temperature sensor and delay-line sensor's outputs are captured at two different temperatures T_1 and T_2, and from the accurate sensor the actual values of T_1 and T_2 can be figured out. *OFFSET'* is adjusted with external temperature reading at startup temperature T_1. And using the temperature information T_1 and T_2, gain *GS'* of the delay-line sensor are solved. This continuous calibration is done with only one delay-line based sensor located close to the accurate sensor on the same chip, and the values for the gain and offset are applied to all sensors. The measurement errors result from four sources. The first two are the nonlinearity of the delay line's temperature characteristic [14] and the deviations among calibrated codes $C(T_1)$. These two sources contribute to less than ±2.0 ºC among different batches, and ±1.0 ºC on die on 65nm FPGA, as reported in [8]. The remaining sources of error are the nonlinearity of the accurate reference temperature sensor and the deviations from the preset gain value before the continuous self-calibration is performed. The error resulted is $DIFF \cdot \Delta GS/GS$ (where $\Delta GS/GS$ is found to be 0.1 via simulation using TSMC's 65nm technology). To keep the error within 3 ºC, *DIFF* must be smaller than 30. The continuous self-calibration is performed with $C(T)$ obtained at T_1 and as its code decrement is larger than *DIFF*.

IV. Prototype Experimental Results

Four different temperature sensor architectures are synthesized on a 65nm Cyclone III FPGA chip. Their specifications and measurements results are as listed in Table I and in Table II, respectively. Each of the architectures is implemented on three different FPGAs, four at a time. To prevent the inverters that made up delay lines from being minimized during compilation in the Quartus™ II software, the connecting wires have to be indicated as (*keep=1*) [3]. The FPGA sensors are tested at 5 °C increment from 20°C to 75°C in an ESPEC™ ETC-3 temperature chamber. A commercial temperature sensor [15] is used as the accurate temperature reference. The delay line sensor resolution is 0.36°C, and the calibration assumes that the accurate temperature sensor has a resolution of 0.125°C. The measured digital outputs with and without the proposed continuous self-calibration, and errors between FPGA and the accurate commercial sensors are as shown in Fig. 6, Fig. 7 and Fig. 8, respectively.

Table I. Prototype Measurement comparison

Prototype no.	Total LE	RO LE	Power (µW)	Errors (ºC)
Traditional short	72	32	8.73	±1.2
Traditional long	295	256	8.56	±0.6
Proposed short (N=2)	60	32	7.88	±1.6
Proposed long (N=5)	380	256	2.91	±1.6

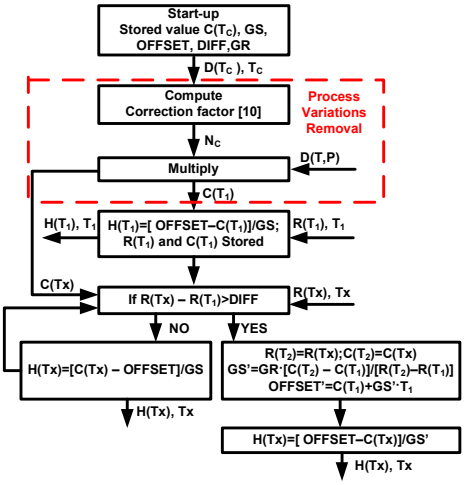


Figure 5. Flow chart for the continuous self-calibration process.

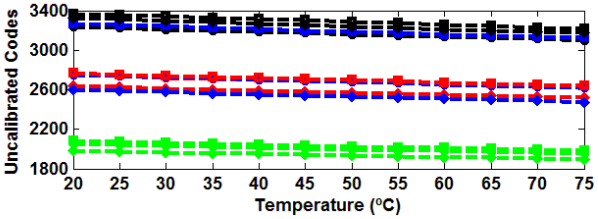
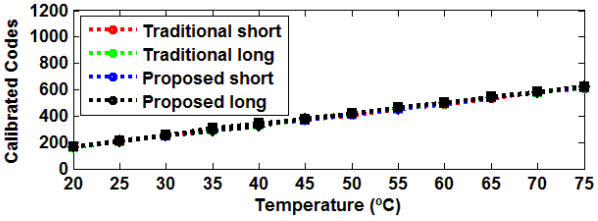
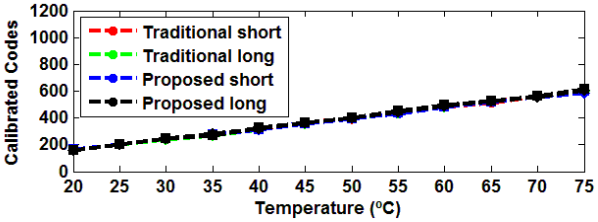


Figure 6. Un-calibrated digital codes from 12 sensors, with 3 for each of the four architectures as listed in Table I.



(a) Calibrated codes without the accurate sensor.



(b) Calibrated codes with the accurate sensor.

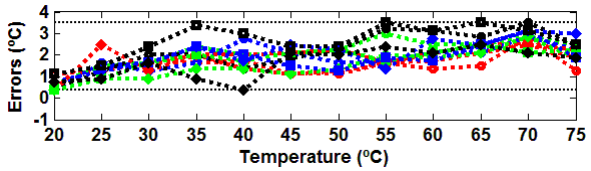
Figure 7. Calibrated digital outputs with (b) and without (a) the accurate sensor.

TABLE II. COMPARISON OF STATE-OF-THE-ART SMART TEMPERATURE SENSORS

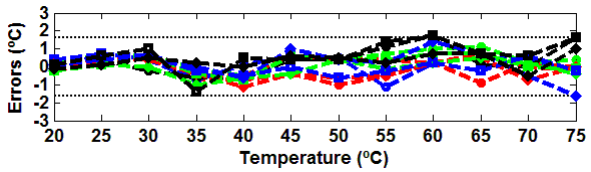
Sensor	Category	Resolution (°C)	Error (°C)	Calibration	Temperature range(°C)	Area (mm^2)	Power (µW)	Conversion time (ms)	Energy per sample (nJ)	CMOS Technology
[2]	Bandgap	0.015	±0.2	One-point	-30~125	0.12	9.2*	100	9200	0.16µm
[4]	CMOS	0.139	-5.1~3.4	auto	0~60	0.01	150	0.1	15	65nm
[5]	CMOS	0.133	-0.7~0.6	One-point	0~100	140LE	175	1	175	0.22/0.18µm
[6]	CMOS	0.66	-1.8~2.3	One-point	0~100	0.12	1200	0.2	240	0.13µm
Proposed N = 2	CMOS	0.125	±1.6	Self-calibration	20~75	60LE	7.88	40	315	65nm
Proposed N= 5	CMOS	0.125	-1.4~1.6	Self-calibration	20~75	380LE	2.91	40	116	65nm

* Not including the ADC required to convert the readings to digital output.

A 63% reduction in power consumption is observed with proposed $N = 5$, and a 10% reduction in power and 17% reduction in area for $N = 2$, as listed in Table I. "Traditional short/long" sensors refer to conventional delay-line sensor using only a counter. "Proposed short/long" sensors use the hybrid counter/pulse position decoder. The continuous self-calibration circuitry occupies 929 LE and consumes 109 µW. It is designed to provide 25 samples per second and with a minimum conversion time of 227 ns. As it performs computation rather than sensing function, the calibration circuit can be placed in a non-critical location and shared among all sensors on the same chip. To handle other sensors, only additional cells for storing the correction factor N_C and a larger multiplexer are needed.



(a) Measurement errors without accurate sensor.



(b) Measurement errors with accurate sensor.

Figure 8. Measured errors from 12 sensors using the proposed self-calibration with (b) and without (a) the accurate sensor.

V. CONCLUSIONS

This paper proposes a power and area efficient all-digital self-calibrated temperature sensor. The experimental prototypes are implemented using 65nm FPGAs. Measurement results verify that the continuous self-calibration technique can effectively remove process variations and reduce power consumption without incurring additional area overhead. The proposed all-digital temperature sensor exhibits resolution of 0.125 °C, errors of less than 1.6 °C and minimum power consumption of 2.9 µW. Furthermore, this design can be fully synthesized and can be adapted to future VLSI/microprocessor designs.

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